A Compact Active Bidirectional Phase Shifter Employing a Highly Isolated Single Gilbert Cell

Uichan Park, *Graduate Student Member, IEEE*, Taeyeong Yoon, *Graduate Student Member, IEEE*, and Jungsuek Oh, *Senior Member, IEEE*

***Abstract*—This letter presents a compact and highly accurate active bidirectional phase shifter (ABPS) with reduced root-mean-square (rms) errors in 28-nm CMOS. The proposed ABPS integrates a transformer-based hybrid coupler (THC) for I/Q signal generation and combining, a bidirectional amplification core, and a Marchand balun-based rat-race coupler (MRRC) for precise signal subtraction and division. A three-stack single Gilbert cell (GC) architecture, arranged in an anti-parallel configuration, enables both amplitude scaling and 180° phase inversion within a compact footprint. An optimized novel electromagnetic (EM) structure is implemented to achieve high port-to-port isolation, ensuring precise phase and magnitude control. The proposed ABPS supports a 6-bit phase shift operation across a full 360° range and demonstrates rms gain and phase errors of 0.36 dB and 2.1°, respectively, in both forward and backward directions. The proposed ABPS was fabricated in a compact area of 1.08 × 0.42 mm^2, consuming 16.2 mW.**

***Index Terms*—Bidirectional, CMOS, Gilbert cell (GC), phase shifter (PS), vector-sum PS.**

I. Introduction

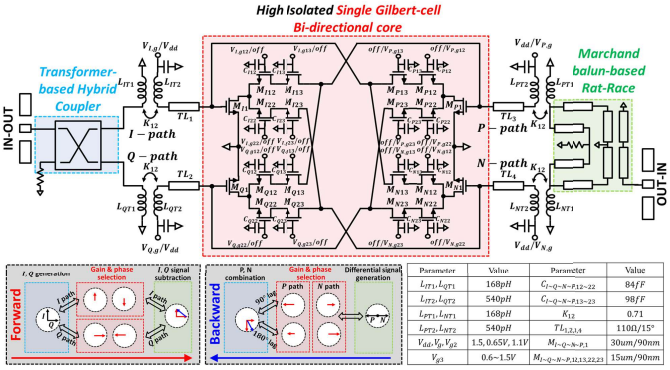
PRECISE beamforming in phased-array systems depends on the performance of phase shifters (PSs). This requirement becomes even more critical in the Ku-band, a key spectrum for emerging 6G communication links. Consequently, developing reliable and area-efficient PSs for this frequency range is imperative. Integrating bidirectional functionality into a single active device is an effective strategy for miniaturization, addressing the significant insertion loss of passive designs [1], [2] and the unidirectional limitation of typically active PSs [3], [4], [5]. Although various active bidirectional PS (ABPS) solutions have been proposed [6], [7], [8], [9], [10], they exhibit notable drawbacks.

The approach in [6], which employs multiple active switches for bidirectional operation, significantly increases the chip area, complicates phased-array integration, and consumes substantial power. Furthermore, although the switchable polyphase filter (PPF) in [7] supports bidirectionality, it encounters challenges in maintaining precise impedance matching across the desired bandwidth with increased operation complexity. An ABPS that realizes low root-mean-square (rms) error by eliminating the switch structure with equalization between input and output impedances is introduced in [8]. However, its primary disadvantage is the large area required by the reflect-type biphase modulator used for 180° phase inversion. Although the 4-bit ABPS in [9] features a compact size, its area increases with the number of bits, and it exhibits a relatively large rms phase error.

Received 19 October 2025; accepted 31 October 2025. This work was supported by Samsung Electronics Company Ltd. *(Corresponding author: Jungsuek Oh.)*

The authors are with the Institute of New Media and Communication (INMC) and the Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, South Korea (e-mail: jungsuek@snu.ac.kr).

Digital Object Identifier 10.1109/LMWT.2025.3629107



Parameter	Value	Parameter	Value
L_{T1}, L_{QT1}	168pH	$C_{I-Q-N-P,12-22}$	84fF
L_{T2}, L_{QT2}	540pH	$C_{I-Q-N-P,13-23}$	98fF
L_{PT1}, L_{NT1}	168pH	K_{12}	0.71
L_{PT2}, L_{NT2}	540pH	$TL_{1,2,3,4}$	110Ω/15°
V_{dd}, V_g, V_{g2}	1.5, 0.65V, 1.1V	$M_{I-Q-N-P,1}$	30um/90nm
V_{g3}	0.6~1.5V	$M_{I-Q-N-P,12,13,22,23}$	15um/90nm

Fig. 1. Schematic of the proposed ABPS with design parameters.

To overcome these challenges, this letter introduces a novel ABPS topology designed to minimize rms gain and phase errors while maintaining a compact size. A highly isolated single Gilbert cell (GC) structure is introduced to enable symmetric bidirectional operation and precise phase control by substantially reducing $0°, 180°$ inversion mismatches. Moreover, mismatches between the I and Q signals are substantially minimized by reducing both direct and indirect coupling effects within the core architecture. The need for a reconfigurable matching network is obviated by adopting a pair of three-stack structures in [8] and [10], thereby enhancing both compactness and reliability.

II. Design of the Bidirectional Active PS

Fig. 1 illustrates the structure of the proposed ABPS. A transformer-based hybrid coupler (THC) is employed for I and Q signals generation and combining, while a novel single-GC architecture with its cells connected in an anti-parallel configuration supporting bidirectional operation is implemented to enable gain adjustment and 180° phase inversion. A Marchand balun-based rat-race coupler (MRRC) is utilized to subtract the I and Q signals during forward operation and to generate differential signals during backward operation.

Fig. 2 shows the principle of forward and backward operation of the ABPS. In the forward operation, the I and Q signals generated by the THC enter the input of each GC, and the desired amplitude and phase are selected through bias adjustment. Finally, the signals are subtracted from each other through the MRRC. Conversely, in the backward operation,

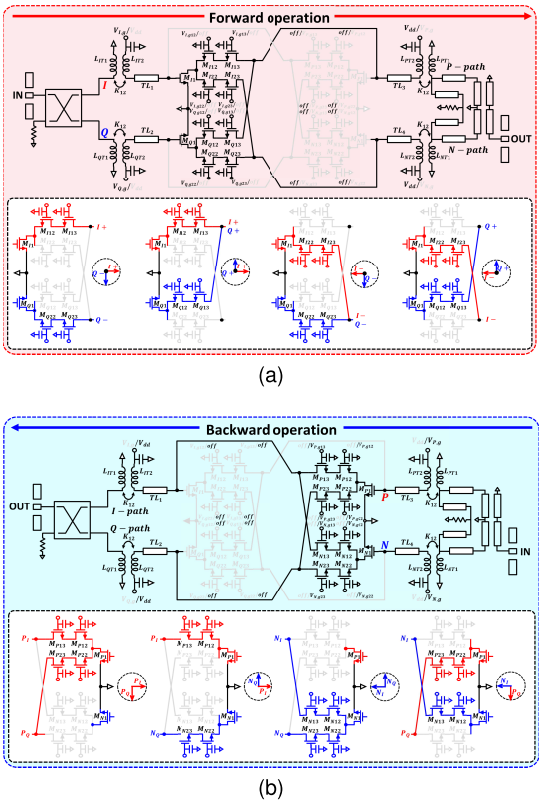


Fig. 2. Operating principles of the proposed ABPS. (a) Forward operation. (b) Backward operation.

the P and N differential signals generated by the MRRC enter the input of each GC. The gain-controlled P and N signals are combined at the THC with a phase difference of 90°.

A. Analysis of the Single GC-Based Bidirectional Core

Fig. 3 shows the proposed bidirectional single GC structure and the effect of signal leakage due to typical node capacitance. The disadvantage of the double GC is that it requires a balun to create the differential signals, which increases chip area and insertion loss [11]. Additionally, its low output impedance complicates the application of the input and output impedance equalization technique from [8] and [10], which is intended to eliminate the need for a reconfigurable matching network. Therefore, the proposed bidirectional core has four ports, with the inputs and outputs of two three-stack single GCs connected in an anti-parallel manner.

A critical challenge in the anti-parallel single-GC architecture is signal leakage caused by parasitic node capacitances, as illustrated in Fig. 3(a). These direct and indirect leakage paths degrade port-to-port isolation. Signals applied to Port 1 should go to Port 3, but in practice, the capacitance causes direct (red solid line) and indirect (red dashed line) leakage paths. The simulation results in Fig. 3(b) and (c) quantify this effect. As shown in Fig. 3(b), when only the forward feed-through capacitance (C_f) increases from 1 to 5 fF, the amplitude difference between the main path (S_{31}) and the leakage path (S_{41}) degrades from 21.7 to 11.2 dB (i.e., isolation degradation). Considering the backward feed-through capacitance (C_b), the amplitude difference degrades from 18.1 to 5.6 dB as capacitance increases, which can be seen in Fig. 3(c). This signal leakage from Ports 3 to 4 significantly degrades phase and amplitude accuracy when I and Q signals

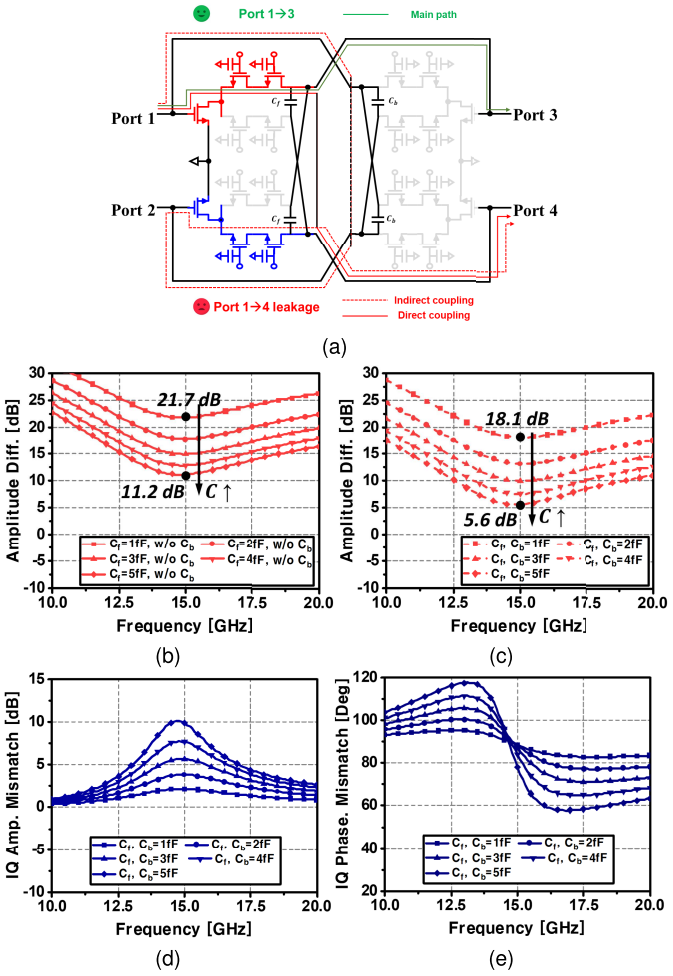


Fig. 3. (a) Proposed bidirectional single GC structure and signal leakage flow due to node capacitance. Amplitude difference between S_{31} and S_{41} as a result of changing (b) C_f only and (c) C_f with C_b. I/Q signal mismatch in the bidirectional single GC structure caused by node capacitance: (d) amplitude mismatch and (e) phase mismatch.

are applied. Fig. 3(d) and (e) represents the amplitude and phase mismatch of I and Q signals at Ports 3 and 4 when ideal I and Q signals are applied to Ports 1 and 2, respectively. Even a small amount of capacitance significantly distorts the I and Q signals; this distortion exceeds the compensation range of the I and Q generation network and fails to address the mismatch caused by gain control in the core. Therefore, a fundamentally effective core layout for coupling reduction is essential to addressing the critical issues.

Fig. 4 depicts the proposed highly isolated core layout and the signal flow diagram under different directions of operation. In the forward case, *I/Q* signals are applied to Ports 1 and 2 and exit from Ports 3 and 4. Conversely, in the backward case, differential signals are applied to Ports 3 and 4 and are routed to Ports 1 and 2 for combining by the THC. The full electromagnetic (EM) simulation results of the core including the matching network can be seen in Fig. 5. It shows that the proposed layout provides about 18 dB of isolation and about 8 dB of gain per path. The 21.4 dB gain control range enables effective *I/Q* and *P/N* signals scaling. The key advantages of this layout are its inherent bidirectional symmetry and minimized parasitic capacitance, which are crucial for high-accuracy phase shifting.

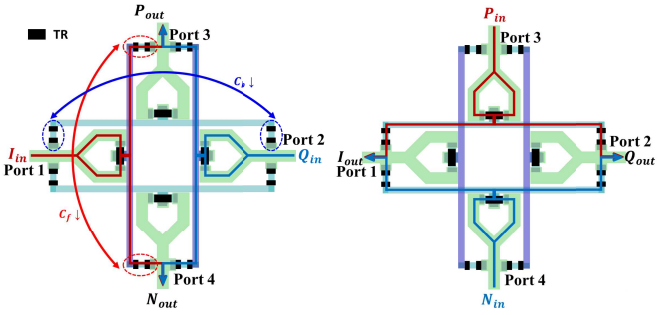


Fig. 4. Proposed bidirectional single GC EM-based structure. Signal flow in (a) forward and (b) backward operation.

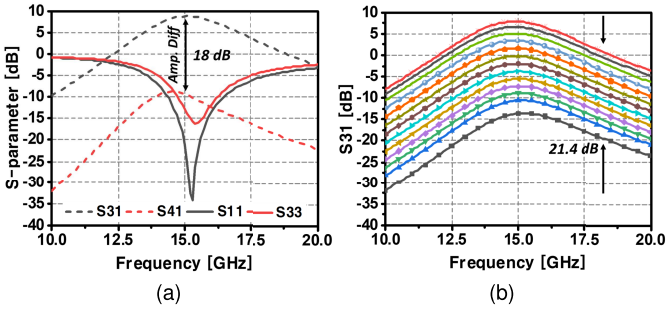


Fig. 5. Full EM results of the highly isolated core including the matching network. (a) Isolation and matching performance. (b) Gain tuning range.

B. Marchand Balun-Based Rat-Race Coupler and Quadrature Hybrid Coupler

For the subtraction of the I and Q signals and the generation of the differential signal, the MRRC shown in Fig. 6(a) is utilized. The all-port match condition was used to minimize the reflections at each port with I and Q signals. To reduce the design area compared to a typical RRC, the Marchand balun shown in Fig. 6(b) was designed using a transformer-based coupler that maximizes the coupling coefficient (0.79), and $90\Omega, 53^\circ$ transmission line (TL) length for THC was adopted to achieve high isolation. Customized THC had a loss of -3.6 dB at 15 GHz with 90° to 91° phase mismatch as shown in Fig. 6(c) and (d). The designed MRRC in Fig. 6(e) shows that all ports are well-matched in the 15 GHz band and have an isolation of about 27 dB. Near 15 GHz, S_{24} and S_{34} show an amplitude of approximately -4.35 dB each, indicating excellent amplitude balance. They also produce accurate differential signals with a phase difference of about 178° to 181° from 12 to 20 GHz.

III. Fabrication and Measurement Results

Fig. 7(a) shows the measurement setup. The S-parameter response was measured using an Anritsu VNA, and two Keysight E36300 units were connected to a PC and the bias was adjusted using a Python program. Fig. 7(b) represents the micrograph of the fabricated chip, which occupies a compact area of approximately 1.08 × 0.42 mm. An IP1dB exceeding -8 dB is measured for both forward and backward operations, with nearly identical linearity performance in both directions.

Fig. 8 presents the measurement results of the proposed ABPS, demonstrating its 6-bit resolution capability. At 14 GHz, the design achieves an average gain of approximately -4.4 and -4.7 dB for both forward and backward operations, with rms phase errors of 0.11° and 0.34°, respectively. Maximum rms gain and phase error of 0.36 dB, 2.1° were measured under bidirectional operation across

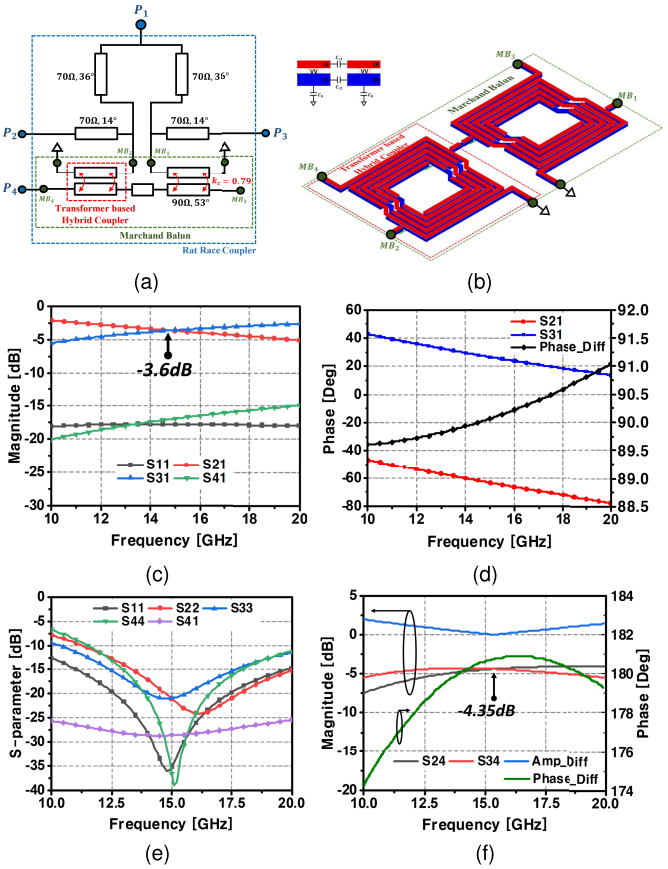


Fig. 6. (a) Schematic of the MRRC. (b) 3-D layout of the Marchand balun. (c) S-parameter magnitude of the THC. (d) Phase. (e) EM-simulated reflection coefficients and isolation of MRRC. (f) Magnitude and phase responses between differential signals.

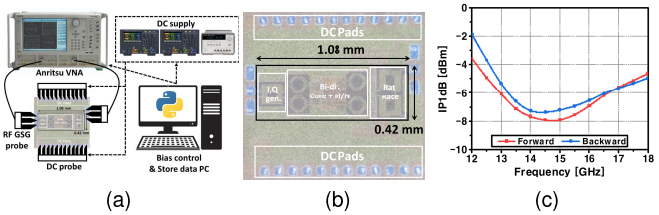


Fig. 7. (a) Measurement setup. (b) Chip micrograph of the proposed ABPS. (c) Measured IP1dB.

TABLE I
Performance Comparison of Recent PSs

Ref	[1] IMS' 23	[2] TVLSI' 25	[3] MWCL' 18	[4] MWCL' 23	[5] RFIC' 24	[6] RFIC' 17	[7] JSSC' 20	[8] IMS' 24	[9] TCASII' 25	This work
Tech	40nm	40nm	0.13um	0.13um	90nm BiCMOS	0.13um SiGe	65nm	28nm	28nm	**28nm**
Topology	VMPS	VMPS	VMPS	VMPS	VMPS	STPS	VMPS	VMPS	STPS	VMPS
BW (GHz)	26–32	26–32	12–18	8–12	2.5–25	8–12	26.5–29.5	13–15	26–30	**13–15**
Passive/Active	Passive	Passive	Active	Active	Active	Active	Active	Active	Active	**Active**
Bi-dir.	O	O	X	X	X	O	O	O	O	**O**
Res. (bit)	6	6	6	6	6	6	6	6	4	**6**
IP1dB (dBm)	14	≥ 13	1~2	6~11	-24~-15	-15	-8	-12.5> / -9.5>	-3.8~-2.15	**>-8 / >-7.5**
Gain Avg. (dB)	-19	-15~-13	-2.5 ~ 1	-3.1~-0.8	> 17	> 11.5	0	-6~-5	0.7	**-4.7**
RMS Phase Error (deg.)	1.8 ~ 2.6	0.4~1.3	1.8 ~ 4	< 0.29	2.7~3.2	< 2.2	< 2	< 2	< 9.5	**< 2.1**
RMS Gain Error (dB)	< 1.2	0.5~0.9	< 0.9	< 0.24	0.9	< 0.9	< 0.4	< 0.6	< 1.1	**< 0.36**
P_DC (mW)	0	0	37.5	90	96	195	20	15.8	40	**16.2**
Area (mm x mm)	0.63 x 0.24	0.67 x 0.27	0.75 x 0.32	1.7 x 0.54	1.31 x 0.52	2.6 x 1.5	0.6 x 0.5	1.25 x 1.08	0.87 x 0.25	**1.08 x 0.42**
FoMA*	39.7	43.2	45.7	62.2	49.7	44.5	44.9	43.4	34.6	**50.6**

$Area_{eff}$ = Area (mm x mm) / λ_c^2 (mm x mm)

*FoMA = $10 \times \log(\frac{BW(\%) \times Res.bits}{RMS\ gain\ error \times RMS\ phase\ error \times Area_{eff}})$

VMPS: Vector modulated phase shifter
STPS: Switch type phase shifter

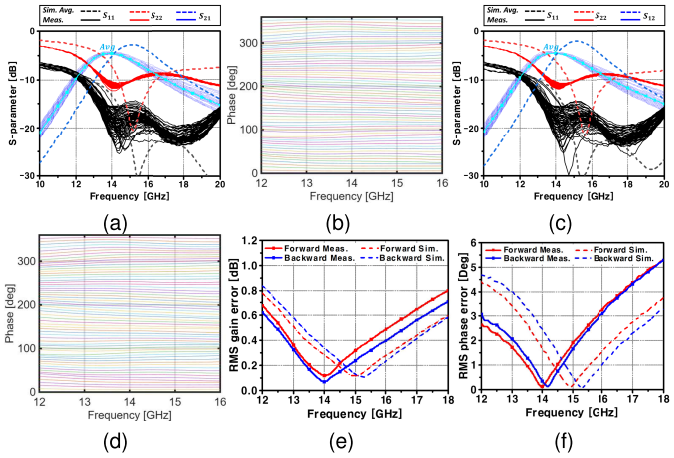


Fig. 8. Measured performance of the ABPS. (a) Forward S-parameters and (b) 64-state phase response. (c) Backward S-parameters and (d) 64-state phase response. (e) RMS gain error and (f) rms phase error.

the 13–15 GHz. Phase response of Fig. 8(b) and (d) clearly demonstrates the consistent phase-shifting performance across all states over the target frequency band. The achieved performance is compared with that of existing PSs in Table I. Compared to existing ABPSs [6], [7], [8], [9], the proposed ABPS shows the second-highest value of FoMA, demonstrating its superiority.

IV. Conclusion

A compact ABPS with high-precision performance has been presented. The proposed design comprises a THC, a bidirectional amplification core utilizing an inversely connected three-stack single GC structure, and an MRRC. By employing the novel EM layout for the bidirectional core, leading to low rms gain and phase errors across the full 360° phase-shifting range. Measurement results validate the symmetric bidirectional performance, with worst-case rms gain and phase errors of 0.36 dB and 2.1°, respectively. The design achieves this performance within a 1.08 × 0.42 mm^2 area while consuming only 16.2 mW, offering a compelling solution for area- and power-constrained phased-array systems.

Acknowledgment

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

References

[1] Y. Tian et al., "A 26–32 GHz 6-bit bidirectional passive phase shifter with 14 dBm IP1 dB and 2.6° RMS phase error for phased array system in 40 nm CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2023, pp. 195–198.

[2] Y. Tian et al., "Design and analysis of a 26–32-GHz 6-bit passive vector modulation phase shifter for CMOS bidirectional transceiver," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 33, no. 3, pp. 673–684, Mar. 2025.

[3] Z. Duan, Y. Wang, W. Lv, Y. Dai, and F. Lin, "A 6-bit CMOS active phase shifter for Ku-band phased arrays," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 7, pp. 615–617, Jul. 2018.

[4] G. Shi, Z. Li, Z. Dai, Z. Li, Z. Hou, and L. Liu, "An X-band 6-bit active vector-modulated phase shifter with 0.29° rms phase error using linearization control technique," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 10, pp. 1482–1485, Oct. 2023.

[5] T. Liang, Z. Hu, O. Hassan, and G. M. Rebeiz, "A 10:1 bandwidth 2.5–25 GHz multi-standard high-linearity 6-bit phased-array receiver front-end with quad-pole I/Q network and 2.7° RMS phase error," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2024, pp. 175–178.

[6] Y. Gong, M.-K. Cho, and J. D. Cressler, "A bi-directional, X-band 6-bit phase shifter for phased array antennas using an active DPDT switch," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 288–291.

[7] J. Pang et al., "A 28-GHz CMOS phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized MIMO for 5G NR," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2371–2386, Sep. 2020.

[8] U. Park, S. Hwangbo, J. Kim, T. Yoon, and J. Oh, "Design of Ku-band bi-directional active phase shifter enabling a low RMS error utilizing switch-less staggered core with the identical in–out matching," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2024, pp. 450–453.

[9] J. Kim, Y. Lee, and B.-W. Min, "A compact Ka-band variable gain phase shifter with bi-directional phase inverting amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 72, no. 1, pp. 133–137, Jan. 2025.

[10] U. Park, S. Hwangbo, J. Kim, T. Yoon, and J. Oh, "A novel switch-less active bi-directional phase shifter with in–out impedance equalization via staggered structure for Ku-band applications," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 5, pp. 2653–2667, May 2025.

[11] Y. Kim, S. Kim, I. Lee, M. Urteaga, and S. Jeon, "A 220–320-GHz vector-sum phase shifter using single Gilbert-cell structure with lossy output matching," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 1, pp. 256–265, Jan. 2015.