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D-Band Stripline Interconnection Using Capped Cavity via Transition

Hyunjin Kim, *Member, IEEE*, and Jungsuek Oh, *Senior Member, IEEE*

***Abstract*— A capped cavity via transition for impedance matching of the stripline interconnection of the multilayered board is proposed at the *D*-band frequency. Equivalent circuits and equations were used to analyze the input impedance of the multilayered via transitions and striplines. The mechanisms that cause narrow bandwidth and high insertion loss were explored. Subsequently, a capped cavity structure for achieving impedance matching between via transitions is proposed. This method allows the capacitance between the via transition and ground planes to be reduced to minimize the reflection coefficient over a wide bandwidth. Measurements were conducted to validate the effects of the proposed method, which demonstrated an increase in bandwidth of over 50 GHz.**

***Index Terms*— *D*-band, multilayer printed circuit board (PCB), via transition.**

I. Introduction

MULTILAYER printed circuit board (PCB) is widely used for packaging and antenna-in-package for millimeter-wave (mmWave) communications [1], [2], [3]. By shifting wireless communications to higher frequencies for increased throughput, the *D*-band (i.e., 110–170 GHz [4], [5], [6]) can be used in future wireless systems. As flip-chip bonding is commonly used in radio frequency integrated circuit (RFIC) module design, interconnection using a stripline and via transitions is also necessary. While the multilayer PCB process is progressing and enabling finer patterns and smaller via holes, the pad and microvia diameters are still large enough to achieve sufficient performance for designing striplines and power dividers. Extensive research efforts have been devoted to modeling structures in multilayered packages and PCBs using full-wave and circuit models [7], [8], [9], [10], [11]. However, despite all the research driven to model via structures, there is a lack of research for modeling and enhancing the performance of stripline and via transitions in the *D*-band. In this letter, we present a stripline with via transition operating at the *D*-band, which is implemented in an advanced multilayer PCB technology that is usually chosen for low-cost, mass production, and interconnection with analog/digital applications.

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The authors are with the Department of Electrical and Computer Engineering, Institute of New Media and Communications (INMC), Seoul National University, Seoul 08826, South Korea (e-mail: hyzinki@snu.ac.kr; jungsuek@snu.ac.kr).

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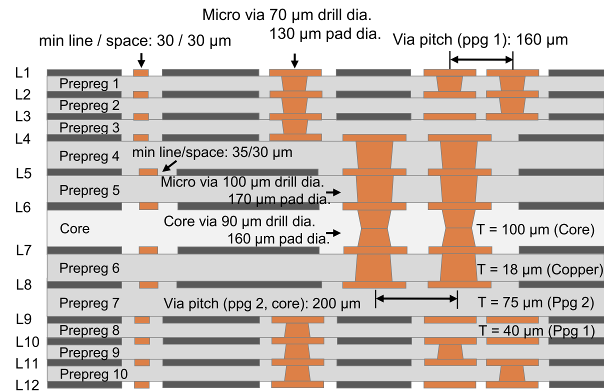

Fig. 1. Stack-up of the multilayered PCB.

II. Stripline Performance Analysis

A. Advanced Multilayer PCB Technology

An advanced multilayer PCB technology, as depicted in Fig. 1, was used in this study. The PCB is composed of a metallization core, preimpregnated (prepreg) material, and laser-drilled microvias. The relative dielectric permittivities of the core and prepreg substrate are 3.4 and 3.2, respectively, and the loss tangent for both the substrates is 0.004. The thicknesses of the core and prepreg layers were 100, 75, and 40 μm, respectively. The minimum diameters of the drilled microvias and the capture pads are illustrated in Fig. 1. Etching technology is currently in progress, with the minimum linewidth and spacing achievable at 25 μm. A margin of 5 μm was adopted to reduce the risk of fabrication errors and misalignment between the microvias and the capture pads.

B. Stripline With via Transition

The ANSYS full-wave electromagnetic (EM) simulation model of the stripline with via transition is depicted in Fig. 2(a), positioned between L9 and L12. The stripline, with width W and length L, is located at L10 and connected from L12 to L10 using microvias and capture pads. The radius of the capture pad is R_P, and the radius of the antipad is R_A.

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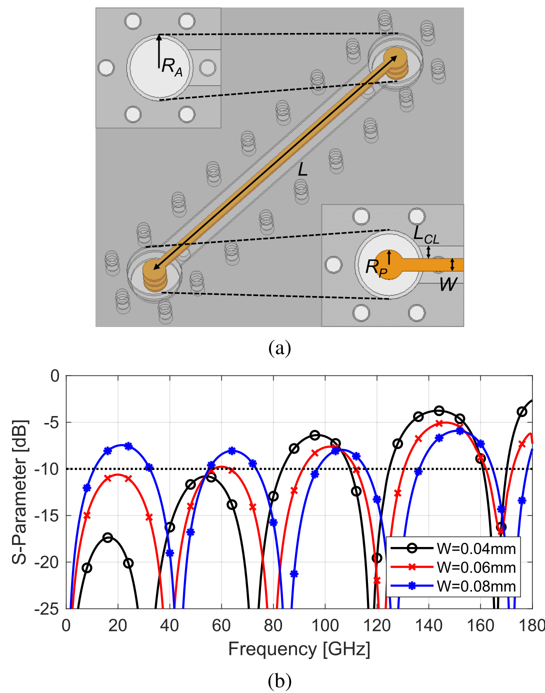

Fig. 2. (a) Stripline simulation model. (b) Simulated results of stripline with via transition.

A diameter of 70 μm was used for the microvia, which represents the minimum value achievable with the drilling process. The reflection coefficients of the stripline with via transition are shown in Fig. 2(b) with $L = 1.7$ mm ($\doteq 1.5\lambda g$), $R_A = 0.18$ mm, $W = 0.5$ mm, and $L_{\mathrm{CL}} = 0.8$ mm. Although the reflection coefficient of the stripline without via transition is smaller than -10 dB for various widths of striplines, the performance deteriorates with the via transition. The reflection coefficient is smaller than -10 dB at 140 GHz when the width is 0.12 mm; however, the bandwidth is narrower than 20 GHz.

C. Equivalent Circuit Model

Fig. 3(a) presents the cross section and parameters of the via transition considered in the multilayer PCB. The capacitance in the model shown in Fig. 3(a) includes the pad barrel-to-plate coaxial capacitance, denoted as C_{BP}, the barrel-to-plate capacitance, denoted as C_{VP}, and the pad-to-plate capacitance, denoted as C_{PP}. C_{BP} can be obtained from [3], while C_{VP} is obtained from [4]. In addition, the capacitance C_{PP} can be calculated using plate capacitance

$$C_{\mathrm{BP}} = \frac{2\pi\varepsilon_r\varepsilon_0 t}{\ln(R_A/R_P)} \tag{1}$$

$$C_{\mathrm{VP}} = \frac{\pi\varepsilon_r\varepsilon_0 h B_0}{\ln(R_A/R_0)} \tag{2}$$

$$C_{\mathrm{PP}} = \frac{\varepsilon_r\varepsilon_0\pi R_P^2}{h} \tag{3}$$

where t and h are the thicknesses of the copper layer and substrate, respectively, and B_0 is a constant coefficient, which can be obtained using Cramer's rule [3]. The multilayer via transitions and striplines in Fig. 2(a) can be simplified to the equivalent circuit model in Fig. 3(c). An effective capacitance, C_S, is used to represent all the capacitances at each layer,

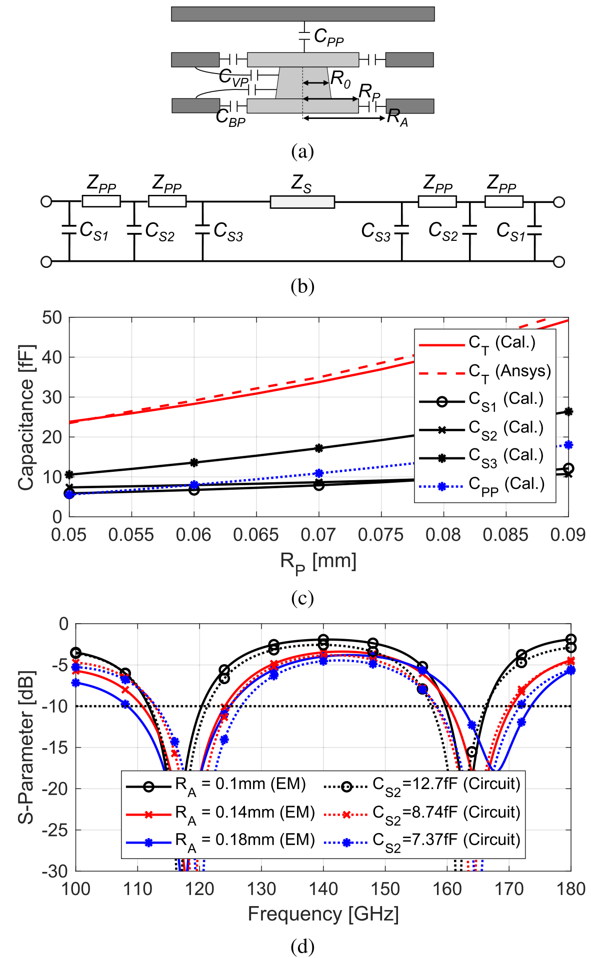

Fig. 3. (a) Illustration of the capacitances of a microvia. (b) Equivalent circuit model. (c) Capacitances as a function of the pad radius. (d) Compared S_{11} of the simulation results.

where $C_{S1} = C_{\mathrm{BP}} + C_{\mathrm{VP}}$, $C_{S2} = C_{\mathrm{BP}} + 2\ C_{\mathrm{VP}}$, and $C_{S3} = C_{\mathrm{BP}} + C_{\mathrm{VP}} + C_{\mathrm{PP}}$. The microvias and striplines are modeled as transmission lines with the impedance of the parallel plate, Z_{PP}, and stripline, Z_S, which were obtained through full-wave simulation. In Fig. 3(c), the total capacitance, C_T, was calculated and compared with the simulated results using ANSYS [7], [8]. The other calculated capacitances, such as C_S and C_{PP}, are also plotted according to R_P, when $R_A = 0.14$ mm and $t = 0.018$ mm. The equivalent circuit model is designed with an ADS circuit simulator, and the results (dashed line) are compared with the full-wave results (solid), as shown in Fig. 3(d). The values used in the circuit simulations are shown in Fig. 3(c). The capacitance, C_{S1}, is fixed at 7.28 fF, as R_A of L12 is determined to be 0.25 mm considering the pitch of the GSG probe (0.15 mm). C_{PP} is also fixed at 9.39 fF, because the minimum R_P is 65 μm. Although the reflection coefficient is enhanced with larger R_A and smaller C_{S2} and C_{S3}, the value is still higher than -10 dB.

III. Proposed Capped Cavity Structure and Validation

The ANSYS EM simulation model of the proposed capped cavity structure, which is designed between L9 and L12, is shown in Fig. 4(a). The design parameters are $W = 0.7$ mm,

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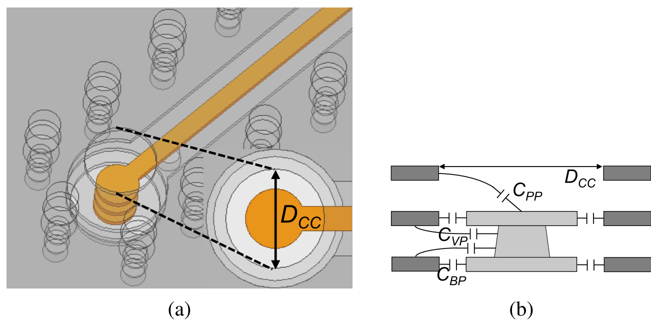


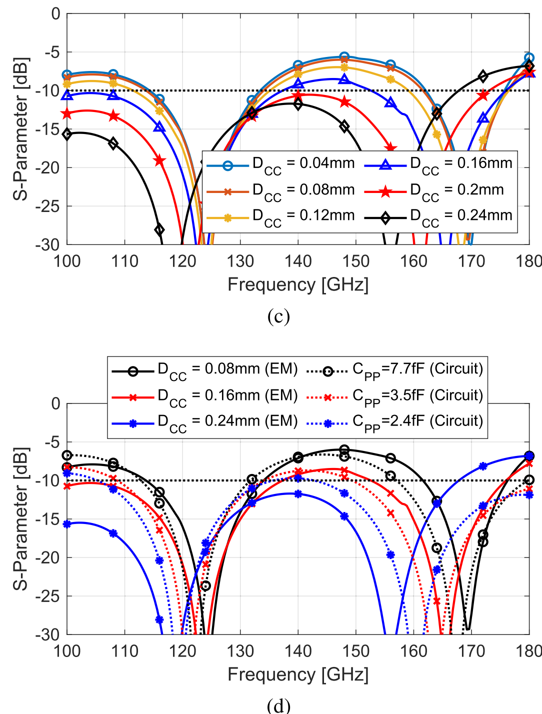
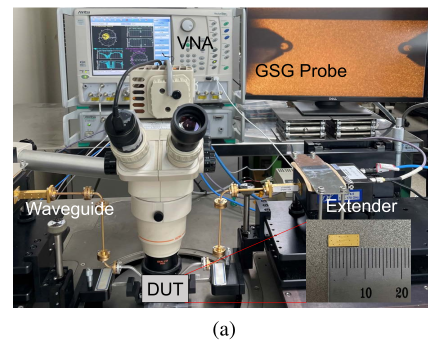


Fig. 4. (a) Full-wave simulation model of the proposed structure. (b) Illustration of the capacitances of a microvia with a proposed structure. (c) Simulated S_{11} versus D_{CC}. (d) Compared S_{11} of the simulation results.



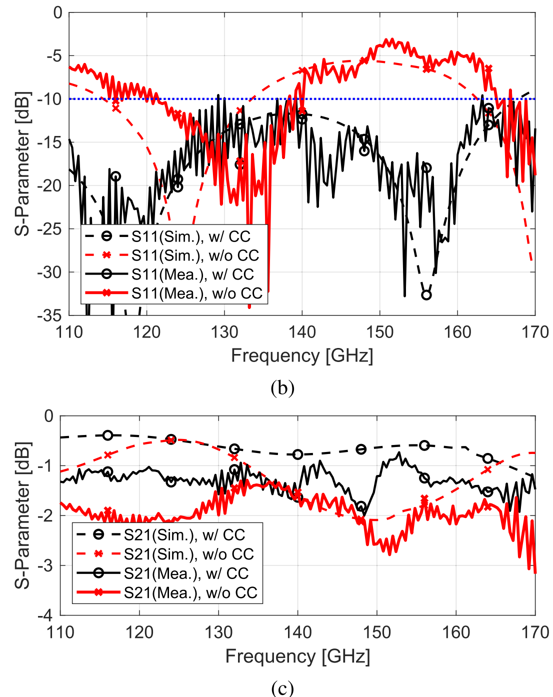


Fig. 5. (a) Measurement environments. (b) Compared reflection coefficients. (c) Compared insertion loss of stripline with and without a capped cavity.

$L = 1.7$ mm, $L_{\mathrm{CL}} = 0.5$ mm, $R_A = 0.15$ mm, and $R_P = 0.065$ mm. Although the proposed model occupies one additional layer, the upper layers of the via transition are typically not usable regions. Fig. 4(b) shows the cross section of the proposed structure, comprising the transition and surrounding microvias. With the proposed structure, C_{PP} can be reduced because the capacitance model can be converted into C_{VP}. Fig. 4(c) presents the EM simulation results for different values of D_{CC}, which can be helpful in determining the dimensions. When D_{CC} is smaller than 0.24 mm, the reflection coefficient is smaller than -10 dB for a wide bandwidth. In Fig. 4(d), the EM and circuit simulation results are compared with the proposed structure. C_{PP} is reduced with larger D_{CC}, and the reflection coefficient can also be improved.

The measured results were obtained in the environment shown in Fig. 5(a) after short–open–load–through calibration. While the measured S_{11} in Fig. 5(b) shows a similar trend as the simulation results, the measured S_{21} in Fig. 5(c) shows an insertion loss that is approximately 0.5 dB higher than that of the simulation. The S_{11} results are compared with and without a capped cavity in Fig. 5(b), and S_{11} with a capped cavity shows a wide -10 dB bandwidth, whereas S_{11} without a capped cavity shows a bandwidth of approximately 10 GHz. The measurements validate the effectiveness of the proposed method, which achieves a bandwidth greater than 50 GHz. In Fig. 5(c), the compared results of the insertion losses are also shown, which are smaller than 2 dB. However, insertion losses without a capped cavity deteriorate due to poor reflection coefficients.

IV. Conclusion

Equivalent circuits and equations have been presented to analyze the input impedance of the multilayer via transitions and striplines. The narrow bandwidth and high insertion loss of the stripline with via transition are also presented using equations and equivalent circuits. Subsequently, a capped cavity structure is proposed as a method to achieve impedance matching of via transitions. This approach reduces the capacitance between the via transitions and ground planes, minimizing the reflection coefficient over a wide bandwidth. Measurements were performed to validate the effectiveness of the proposed method.

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