# Liquid-Crystal-Based *X*-Band Reactively Loaded Reflectarray Unit Cell to Reduce Reflection Loss

Hogyeom Kim, Jongyeong Kim, and Jungsuek Oh

***Abstract*—This letter presents a novel design of a nematic liquid-crystal (LC)-based *X*-band reactively loaded reflectarray unit cell (RLRUC) to reduce reflection loss. The reflection loss of an LC-based reflectarray unit cell (RUC) can be reduced by increasing the thickness of the LC or the superstrate. However, in the conventional RUC, the superstrate thickness has little impact on the reflection loss due to the absence of a contribution to the actual input impedance. The reflection loss can be significantly reduced by adding an additional metallic patch onto the top of the superstrate, which serves as a reactive load. The reflection loss is analyzed by an equivalent circuit model in this letter. For the measurements, a $1 \times 2$ array of unit cells is introduced. Metallic vias shielding around the unit cell array is embedded into the substrates to substitute for a metallic wall. In addition, a simple bias configuration is achieved by inversely arranging the substrates. The RLRUC achieves a dynamic phase range of 240° with a reflection loss of only 1.5 dB. Compared to earlier work which reported an LC-based RUC that operated on the *X*-band, the proposed design achieves extremely low reflection loss.**

***Index Terms*—Liquid crystal (LC), reactively loaded reflectarray unit cells (RLRUC), X-band reconfigurable unit cell.**

## I. Introduction

REFLECTARRAY antennas consist of two-dimensional (2-D) periodic patterns printed on a grounded substrate. These have several advantages, including their ease of fabrication, planarity, and low cost. Recently, many researchers have been actively studying electronically controllable reflectarrays, which operate on the mmWave band [1]–[4]. The liquid-crystal (LC)-based reflectarray is a reflectarray that radiates scattered waves toward a desired direction as the permittivity of the LC changes. The value of the permittivity of the LC can be controlled by biasing the dc voltage or ac voltage at a low frequency [4]. Metallic layers adjacent to the LC are connected to the bias line. When dc or low-frequency ac bias is applied to the metallic layers, *E*-fields perpendicular to the dipoles of the LC are generated, leading to a change in the permittivity of the LC. The main advantage of the LC is the continuous reconfigurability, by which the value of the permittivity can be controlled proportionally to the applied voltage level.

There have been numerous works on LC-based reflectarrays that operate on various frequency bands [5]–[10]. These works present a LC-based reflectarray unit cell (RUC) with high reflection loss due to the nature of the LC. Specifically, prior works on the *X*-band have reported an LC-based RUC having higher reflection loss than those on other frequency bands [5], [6]. This is possible because the impedance condition of the unit cell is close to an absorber condition and not to a reflectarray condition. It is well known that the reflection loss and phase dynamic range are important factors when designing a reflectarray antenna for high efficiency [11]. The reflection loss of the unit cell based on a lossy medium such as LC can be reduced by optimizing the impedance [12].

Numerous LC-based RUC structures in the literature consist of three dielectric layers, the substrate, spacer (LC layer), and superstrate [10], [13], [14]. The metallic layers in these works are placed on the LC layer only [13]. The reflection loss of these conventional RUCs can be reduced by increasing the thickness of the LC or the superstrate. However, the thicker the LC, the more the rising time of the LC increases proportionally to the square of the thickness [15]. Therefore, the reflection loss should be reduced by changing the superstrate thickness. A major problem with these types of unit cells is that increasing the superstrate thickness slightly reduces the reflection loss due to the absence of a contribution to the actual input impedance of the unit cell.

The main purpose of this letter is to reduce the reflection loss of the RUC within an acceptable phase dynamic range by increasing the superstrate thickness. In this letter, an LC-based reactively loaded reflectarray unit cell (RLRUC) with low reflection loss on the *X*-band is presented. It is demonstrated that a significant reduction of the reflection loss can be achieved by employing an additional metallic patch onto the top of the superstrate, which works as a reactive load. This effect is analyzed by assessing the equivalent circuit (EC) and by means of a full-wave EM simulation conducted using ANSYS HFSS.

Table I shows comparisons of the maximum reflection loss and LC thickness in prior works and this work based on a LC-based RUC. Although the thickness of the LC of the proposed RLRUC is smaller than that of the RUCs in other works, the RLRUC shows a low reflection loss. Here, a $1 \times 2$ RLRUC array is designed to measure the proposed design considering the aperture of the waveguide. In order to emulate an infinite periodic structure, i.e., a Floquet simulation, metallic vias shielding the

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TABLE I
COMPARISONS OF THE REFLECTION LOSS AND LC THICKNESS

| Frequency [GHz] | Max. Reflection loss [dB] | LC thickness [$\lambda_0$] | Reference |
|---|---|---|---|
| 10 | 38 | 0.0167 | [5] |
| 24 | 7 | 0.04 | [7] |
| 104 | 7 | 0.026 | [2] |
| 9 | 1.5 | 0.0075 | This work |

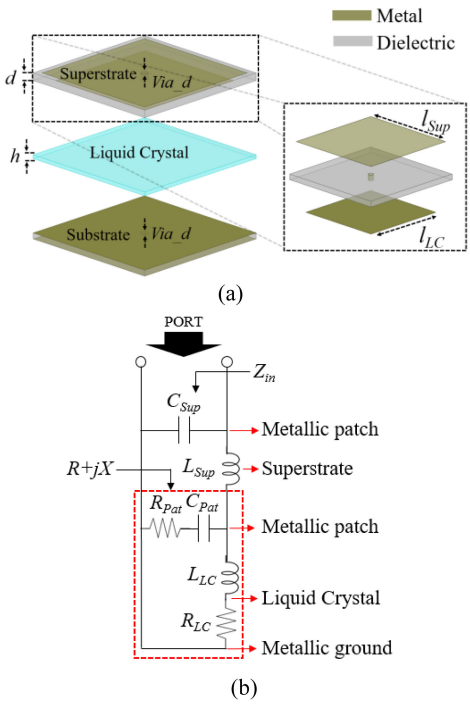


Fig. 1. (a) Exploded image of the designed RLRUC. (b) Corresponding EC model.

1 × 2 RLRUC array are embedded into the dielectrics. The measured results are in good agreement with the simulation results.

## II. LC-BASED LOW-LOSS RLRUC DESIGN

In this section, the reflection loss and phase dynamic range of the RLRUC are discussed. The performance of the RLRUC is compared with that of the conventional structure of a LC-based RUC. In this letter, a unit cell consisting of only a metallic patch and ground adjacent to the LC layer with three dielectrics represent the conventional RUC. Also, an EC of the RLRUC is analyzed for a parametric study. An EM simulation of the unit cell is conducted, specifically a Floquet simulation in HFSS. The 1 × 2 RLRUC array is designed for the measurement of the RLRUC. Metallic vias are embedded into the substrates to replace the metallic wall. This waveguide simulator suitably represents a Floquet simulation. Fig. 1(a) shows an exploded view of the RLRUC. The top and the bottom sides of the superstrate consist of metallic patches. The metallic patch on the top of the superstrate serves as a reactive load.

Metallic grounds are placed on the top and bottom sides of the substrate. Taconic TLY-5 and FR4 are chosen as the superstrate and substrate, respectively. The relative permittivity of the LC ($\varepsilon'_{LC} + j\varepsilon''_{LC}$) has a complex value due to its loss feature. Based on the datasheet, the tunable range of the dielectric constant of the LC used in this letter is expected to be 2.5–3.5, and the corresponding loss tangent decreases from 0.012 to 0.0064. In order to focus electric static fields toward the LC layer when a bias voltage is applied, a single via is embedded into the superstrate. Also, a single via is embedded into the substrate for the ease of ground bias. Assuming there is no coupling between the interlayer metallic patches, the corresponding EC model of the RLRUC is shown in Fig. 1(b). The metallic patches and the substrate in the red box are modeled by the series $R_{\mathrm{Pat}}$, $C_{\mathrm{Pat}}$, and the series $R_{\mathrm{LC}}$, $L_{\mathrm{LC}}$, respectively [12]. The geometric parameters of the metallic patches in the medium upon which electromagnetic waves normally impinge are expressed respectively as [16]

$$C_{\mathrm{Sup}} = \varepsilon_0 \varepsilon_{\mathrm{eff1}} \frac{2D}{\pi} \ln\left(\csc\frac{\pi(D - l_{\mathrm{Sup}})}{2D}\right) \tag{1}$$

$$C_{\mathrm{Pat}} = \varepsilon_0 \varepsilon_{\mathrm{eff2}} \frac{2D}{\pi} \ln\left(\csc\frac{\pi(D - l_{\mathrm{LC}})}{2D}\right). \tag{2}$$

$l_{\mathrm{Sup}}$ and $l_{\mathrm{LC}}$ represent length of the top patch and the bottom patch on the superstrate, respectively. Assuming low-loss to the superstrate, the effective permittivity outcomes of $C_{\mathrm{Sup}}$ and $C_{\mathrm{Pat}}$ can be correspondingly expressed as [17]

$$\varepsilon_{\mathrm{eff1}} = \frac{\varepsilon_{Sup} + 1}{2} \tag{3}$$

$$\varepsilon_{\mathrm{eff2}} = \frac{\varepsilon_{\mathrm{Sup}} + \varepsilon'_{\mathrm{LC}}}{2}. \tag{4}$$

Here, $\varepsilon_{\mathrm{Sup}}$ and $\varepsilon'_{LC} + j\varepsilon''_{LC}$ are the relative permittivity values of the superstrate and the LC, respectively. The resistance of the metallic patch adjacent to the LC is expressed as

$$R_{\mathrm{Pat}} = \frac{-\varepsilon''_{\mathrm{LC}}}{\omega_0 C_{\mathrm{Pat}}(\varepsilon'_{\mathrm{LC}} + \varepsilon'_{\mathrm{Sup}})}. \tag{5}$$

In this equation, $\omega_0$ represents the operating frequency of the RLRUC. The parameters of the grounded LC slab at normal incidence can be expressed as follows:

$$L_{LC} = \frac{Z_0}{\omega_0 \sqrt{\varepsilon'_{LC}}} \left[\tan(k_0 h \sqrt{\varepsilon'_{LC}})\right]$$

where $k_0$ is the free-space propagation, $Z_0$ is the characteristic impedance of free space, and $h$ is thickness of the LC. The resistance of a lossy grounded dielectric slab is derived by

$$R_{\mathrm{LC}} = \frac{Z_0}{\sqrt{\varepsilon'_{\mathrm{LC}}}} \left[\frac{\varepsilon''_{\mathrm{LC}}}{2\varepsilon'_{\mathrm{LC}}} \tan(k_0 h \sqrt{\varepsilon'_{LC}}) - k_0 h \frac{\varepsilon''_{\mathrm{LC}}}{2\varepsilon'_{\mathrm{LC}}} \times (1 + \tan^2(k_0 h \sqrt{\varepsilon'_{\mathrm{LC}}})\right]. \tag{6}$$

The maximum reflection loss occurs at resonance defined as [12]

$$\Gamma \approx \frac{\mathrm{Re}\{Z_{\mathrm{in}}\} - Z_0}{\mathrm{Re}\{Z_{\mathrm{in}}\} + Z_0}. \tag{7}$$

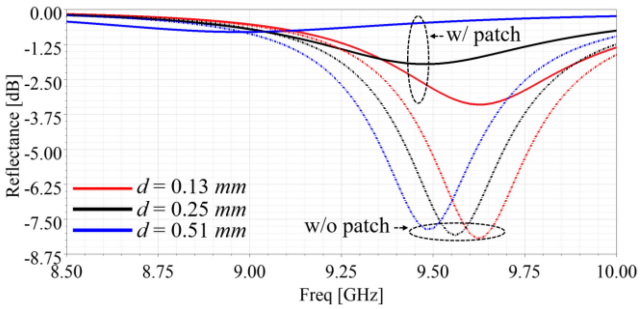


Fig. 2. Reflection losses (a) without (w/o) a metallic patch (dashed lines) and (b) with (w/) a metallic patch (solid lines) on top of the superstrate for various superstrate thickness $d$ (cell size $= 10 \times 10$ mm).

Thus, if the real input impedance of the RLRUC increases, the reflection loss can be reduced.

Fig. 2 presents the reflection loss of with and without metallic patches on top of the superstrate for various superstrate thicknesses. The cases without and with metallic patches represent the conventional and the proposed unit cell structure, respectively. For the case without metallic patches, represented by dashed lines (w/o $C_{\mathrm{Sup}}$), that is, the conventional structure, the input impedance can be expressed by

$$Z_{\mathrm{in}} = R + j(X + \omega_0 L_{\mathrm{Sup}}). \tag{8}$$

Here, $R + jX$ denotes the equivalent impedance in the red box, as shown in Fig. 1(b). The inductance of the superstrate is modeled by

$$L_{\mathrm{Sup}} = \mu_0 * d. \tag{9}$$

In this equation, $\mu_0$ and $d$ are the permeability and the superstrate thickness, respectively. The added term $j\omega_0 L_{\mathrm{Sup}}$ affects the resonance frequency shift. Although the actual impedance is not affected by the inductance in (8), the reflection loss is slightly reduced due to the interlayer coupling. For the case w/ metallic patches, represented by solid lines (w/ $C_{\mathrm{Sup}}$), that is, the RLRUC, there are certain advantages of employing the metallic patches on top of the superstrate. First, the operating frequency can be reduced due to the increase of the superstrate thickness, leading to the miniaturization of the unit cell. Second, the reflection loss can be significantly reduced given the increase in the superstrate thickness. After simple algebra, the input impedance of the RLRUC can be expressed by

$$\mathrm{Re}\{Z_{\mathrm{in}}\} = \frac{R}{(\omega_0 C_{\mathrm{Sup}} R)^2 + (\omega_0^2 C_{\mathrm{Sup}} L_{\mathrm{Sup}} + \omega_0 C_{\mathrm{Sup}} X - 1)^2}. \tag{10}$$

$L_{\mathrm{Sup}}$ now can contribute to the input impedance, leading to a significant reduction of the reflection loss due to the increased superstrate thickness, as shown in Fig. 2. As the superstrate thickness increases, the inductance increases, leading to a reduction of the denominator in (10). Then, the actual impedance will increase.

Fig. 3 depicts the real and imaginary impedances in the cases with and without the metallic patches for various superstrate thicknesses. The solid lines and dashed lines represent the results of the full-wave simulation and the EC model analysis,

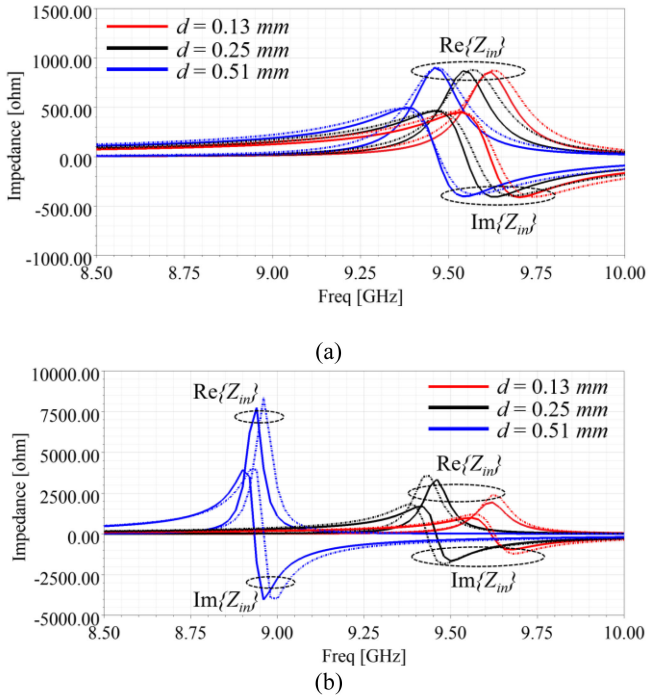


Fig. 3. Real and imaginary impedances (a) w/o and (b) w/ a metallic patch, respectively. Solid lines: full-wave simulation and dashed lines: EC model.

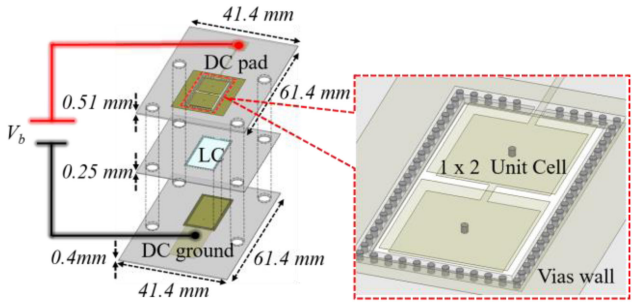


Fig. 4. Exploded view of the $1 \times 2$ RLRUC sample for measurement (cell size $= 10 \times 10$ mm, $l_{\mathrm{Sup}}$: 8.7 mm, and $l_{\mathrm{LC}}$: 9 mm).

respectively. In the w/o case, the real and imaginary impedances show few changes as the superstrate thickness increases. The impedances of the case w/ metallic patches, however, shows significant changes as the superstrate thickness increases. Fig. 4 depicts the $1 \times 2$ RLRUC sample used for the measurement. The diameter of the metallic via is 0.5 mm. The space between the via walls is 1 mm due to the fabrication limit. The size of the superstrate, the spacer (LC), and the substrate are set to 0.51, 0.25, and 0.4 mm, respectively. The dc pad and dc ground have no impact on the performance of the RLRUC. Bias voltage $\mathrm{V_b}$ is applied to the dc pad and ground for reconfigurability of the RLRUC. Three dielectrics are drilled $(4.2\varphi)$ to connect the WR-90, transition, and the RLRUC. The transition is introduced to mitigate the impedance discontinuity between the waveguide and the RLRUC (from $22.8 \times 10.1$ to $20 \times 10$ mm). The RLRUC sample for the measurement is designed as a $1 \times 2$ array to match the size of the WR-90 waveguide.

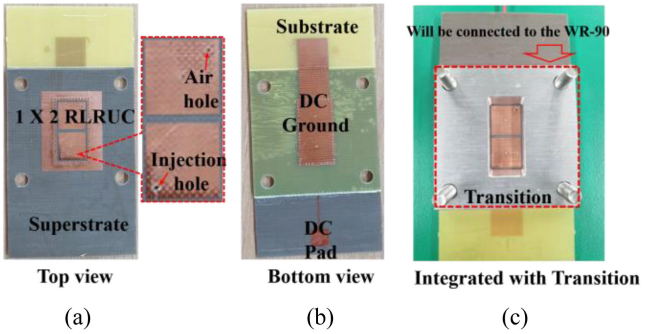


Fig. 5. (a) Top view and (b) bottom view of the fabricated sample and (c) top view of the transition integrated sample.

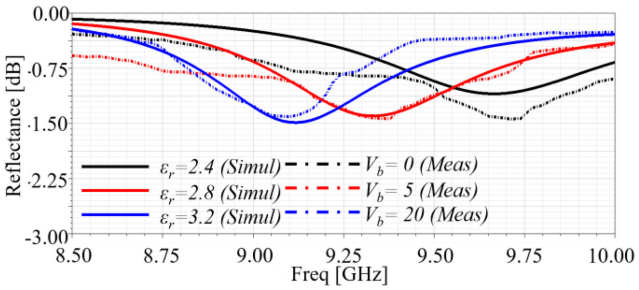


Fig. 6. Comparison between simulated and measured magnitude frequency responses of the RLRUC.

Also, metallic vias are embedded into each layer to emulate an infinite periodic arrangement.

## III. Fabrication and Measurement Results

In this section, the fabricated sample and measured results of the RLRUC are discussed. The fabricated RLRUC sample is shown in Fig. 5. The top and bottom views of the fabricated sample are shown in Fig. 5(a) and (b), respectively. In Fig. 5(a), the injection hole is introduced to inject the LC into the RLRUC. Air slowly escapes from the air hole when the LC is injected into the injection hole. In Fig. 5(b), the dc ground and dc pad are connected to the bias line from the dc supply. The transition is stacked onto the RLRUC, as shown in Fig. 5(c), with four screws. Owing to the transition and metallic via walls, the wave from the WR-90 only impinges upon the $1 \times 2$ RLRUC array. The fabricated sample is measured using the WR-90 waveguide. Fig. 6(a) shows a comparison between the simulated and measured magnitude frequency responses of the RLRUC. The solid lines and the dashed lines represent the simulated and measured results, respectively. By setting the angle of incidence as

$$\theta = \sin^{-1}\left(\frac{\lambda}{\lambda_c}\right) \tag{11}$$

the simulated results according to a Floquet simulation can be matched to measured results from the waveguide simulator [18].

Fig. 7 shows the measured magnitude and the phase responses versus the bias voltage level at 9 GHz. These results are measured with a vector network analyzer that measured $S_{11}$. Saturation occurs above 13 V, as shown in Fig. 7.

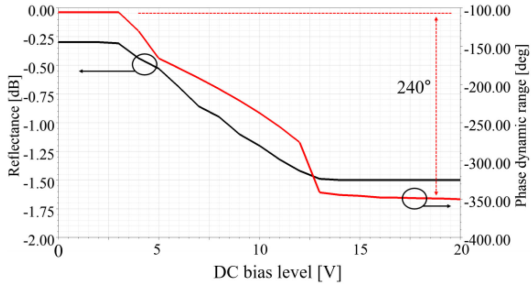


Fig. 7. Measured magnitude (black line) and phase responses (red line) versus the dc bias level at 9 GHz.

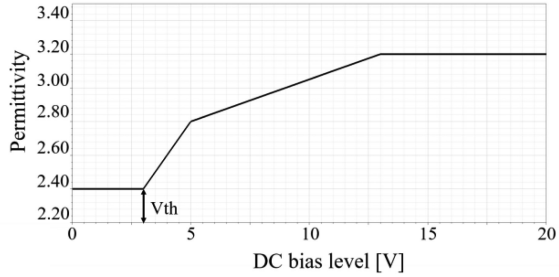


Fig. 8. Effective dielectric constant of LC as a function of the dc bias level at 9 GHz.

A phase dynamic range of 240° can be achieved by applying dc bias voltage from 0 to 20 V, as shown in Fig. 7. Fig. 8 shows the measured dielectric constant of the LC as a function of the dc bias level by comparing the simulated $S_{11}$ at 9 GHz as a function of the dielectric constant of the LC and the measured $S_{11}$ as a function of the dc bias voltage. The range of the applied voltage level is 0–20 V, and the threshold voltage is about 3 V. The error range of the dielectric constant between the datasheet and the measured results arises due to differences in the electric field distribution where the dc bias voltage is applied. The waveguide and the transition affect the electric distribution, resulting in an error between the datasheet and the measured results.

## IV. Conclusion

An LC-based RLRUC on the *X*-band is presented in this letter to reduce the reflection loss. The proposed RLRUC shows a significant reduction of the reflection loss compared to other published structures that operate on the *X*-band [5], [6]. A corresponding EC of the RLRUC is introduced to explain why the reflection loss can be lowered in the RLRUC. Low reflection loss can be achieved by adding an additional patch onto the top of the superstrate, which serves as a reactive load. The added patch affects the actual input impedance. Consequently, the superstrate thickness can affect the reflection loss. The RLRUC structure is fabricated in the form of a $1 \times 2$ array for measurements with a WR-90 waveguide. The results were measured by a waveguide simulator and compared to the simulated results by a Floquet simulation in HFSS. The measured results are in agreement with the simulation results and demonstrate the good performance of the proposed RLRUC.

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