A Novel Switch-Less Active Bi-Directional Phase Shifter With In–Out Impedance Equalization via Staggered Structure for *Ku*-Band Applications

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***Abstract*— In this article, a switch-less vector-sum active bi-directional phase shifter (VABPS) is proposed that operates in the *Ku*-band and has low root-mean-square (rms) gain and phase errors with low power consumption. While conventional amplification structures address the varying input and output (IO) impedances in bi-directional operation by adding a reconfigurable matching network, this article presents the equivalent IO matching technique that eliminates the need for any additional variable matching network. The three-stack switch-less staggered structure is unveiled to facilitate identical IO impedances. This feature significantly enhances the reliability of bi-directional phase shift operations by mitigating both gain and phase errors. In addition, the optimized transformer-based hybrid coupler (HC) is adopted for generating accurate *I* and *Q* signals, followed by a biphase modulator (BM) that creates accurate 180° phase inversion of *I* and *Q* signals by resolving the nonideal effect of the HC. The proposed VABPS supports a 6-bit resolution with a phase shift range of 360° and has an rms phase error of less than 2.4° and a gain error of less than 0.55 dB in 13–15 GHz. The suggested VABPS consumes about 15.8 mW. The chip is fabricated in a standard 28-nm CMOS process and the core area is 1.25 × 1.08 mm^2 including the pad.**

***Index Terms*— Bi-directional, biphase modulator (BM), CMOS, hybrid coupler (HC), input and output (IO) impedance, phase shifter (PS), vector-sum PS.**

I. Introduction

IN PHASED array systems, attaining accurate beamforming requires an intricate phase shifter (PS) design with a high phase shift accuracy [1], [2], [3], [4]. Numerous PS methods, including switch-type PS (STPS) [5], [6], [7], [8], [9], [10], reflection-type PS (RTPS) [11], [12], [13], [14], [15], [16], and vector-sum PS (VSPS) [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], that operate in the widely used mm-wave bands of 28 and 39 GHz, have been created and explored. In addition to mm-wave bands, the *Ku*-band is used for existing satellite communications and is a strong candidate for the 6G Upper-mid (7–24 GHz) spectrum [32], [33], [34], which is considered essential for general communication linkages. In particular, the 7–16-GHz band has the advantage of high throughput and wide coverage [34] and is regarded as a candidate band for 6G mobile. Consequently, it is imperative to design a PS that has excellent reliability and takes up a small area in this *Ku*-band, such as the example designed in [35] and [36].

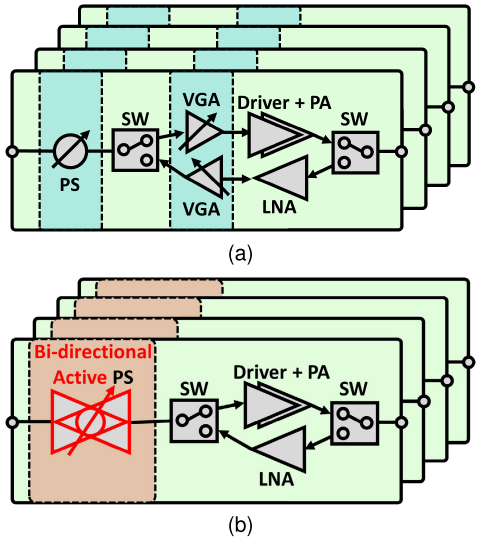

Fig. 1. Block diagram of the (a) conventional bi-directional phased array and (b) proposed bi-directional phased array.

Fig. 1(a) shows the block diagram of a conventional bi-directional phased array. The operation of the transmit (Tx) and receive (Rx) ends is controlled through a switch, and only one PS is placed before the switch to reduce the size of the circuit. In addition, since the phase shift block must support both receiving and transmitting operations, passive-type PS is widely utilized. However, significant losses that are attributed to the passive components, are compensated or adjusted by placing variable gain amplifiers (VGAs) in the Tx and Rx paths. A typical VGA only supports uni-directional operation due to its amplification function, increasing chip

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area as it requires separate VGAs for the Tx and Rx paths. The proposed bi-directional phased array scheme is shown in Fig. 1(b). In this article, we propose the active bi-directional PS (ABPS) that combines the functions of two VGAs and PS used in Fig. 1(a) into one and enables bi-directional operation, which can significantly reduce the overall chip area.

There are two types of PSs: passive PSs [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [25], [26], [27], [36] and active PSs [17], [18], [19], [20], [21], [22], [23], [24], [28], [29], [30], [37], [38], [39]. Passive PS offers several advantages such as zero power consumption, high linearity, and support for bi-directional operation. However, STPS suffer from a significant drawback in their inability to adjust gain. An alternative, the passive VSPS [25], [26], [27], [31], [36] can adjust gain, but this capability comes with the tradeoff of substantial losses and the requirement for an additional amplification architecture. As a result, active PS, which has the advantage in terms of gain, is often used. In particular, active VSPS (AVSPS) has been widely studied because it has good performance in various aspects such as gain, chip area, and root-mean-square (rms) error, but its bi-directional operation is limited due to the intrinsic structural limitations of the active structure. Therefore, to address this issue, a study on the structure and operation of an ABPS was presented in [30], [38], and [39]. However, the currently existing research on this topic is insufficient.

Combining VGAs and PSs in the Tx and Rx paths of a traditional RF transceiver is crucial to minimize the PS block's footprint while concurrently enabling bi-directional operation. Different implementations of ABPSs that perform these functions will vary in performance and complexity. In the case of [39], an active switch is utilized to achieve bi-directional operation. This method has a high gain, but it has the disadvantages of not being able to adjust the gain due to the conventional STPS method, consuming very large dc power, and having a large chip size.

In the case of [30], a switchable poly-phase filter (PPF) that can be used in both the PPF mode and the adder mode is utilized. However, this method requires a varactor for additional matching compensation and a transistor (TR) switch for bi-directional signal synthesis operation due to the differing output impedance of the adder mode and the PPF mode. Consequently, this increases operational complexity, introduces loss, and limits the bandwidth. To solve the aforementioned problems of reduced bandwidth and matching accuracy, [38] adopted a switchable PPF with TR switches, but eliminated the varactor and used a reconfigurable network with additional switches to achieve relatively wideband matching. However, even though the reconfigurable network is configured using additional switches, performance deterioration occurs because of the inaccurate wideband matching. Critically, the limitation of this study on the PS is that it presents only simulation results without any corresponding measurement results.

In this article, switch-less vector-sum ABPS (VABPS) operating in the Ku-band with low rms gain and phase error is proposed. The proposed VABPS utilizes only the properties and routing of stacked TRs to create the identical input and output (IO) impedance, eliminating the need for additional reconfigurable networks and switches. In particular, through an accurate matching procedure, it shows symmetrical performance in terms of gain and rms errors during forward and backward operation with low power consumption. In addition, optimization and improvement methods for blocks such as I, Q generator, and biphase modulator (BM) that comprise VABPS are introduced to show the overall circuit design process.

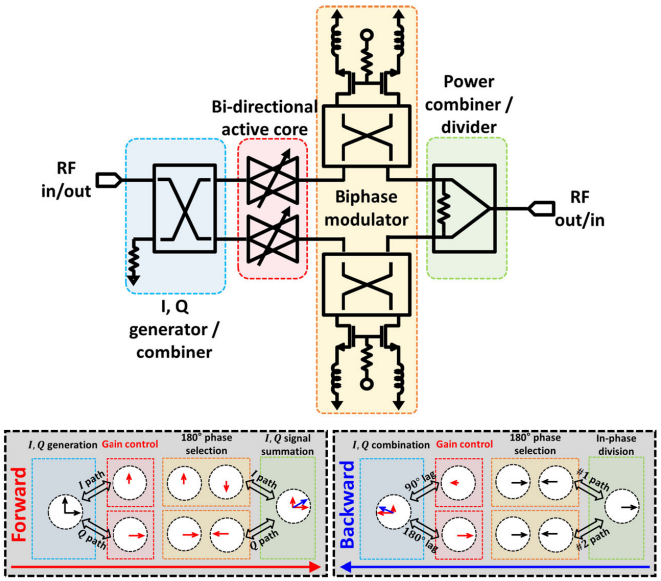

Fig. 2. Block diagram of the proposed switch-less vector-sum active bi-directional PS.

The article is structured as follows: Section II presents the proposed VABPS architecture. Section III addresses the design methodology of the proposed bi-directional core. An explanation of the other blocks of the VABPS with a full schematic is provided in Section IV. In Section V, measurement results are presented. Section VI concludes with a comparison to comparable state-of-the-art PSs.

II. Architecture of the Proposed Bi-Directional PS

The operating principles of the proposed VABPS are demonstrated in Fig. 2. For forward actions, I and Q signals are produced via a transformer-based hybrid coupler (HC), and gains are adjusted for each path by a proposed bi-directional amplification structure that has identical IO impedances. The signals are produced in a Wilkinson power combiner (WPC) that reduces reflections after passing through an RTPS-based low-loss BM that supports 180° phase inversion.

In the backward operation, the input signal is separated in phase by the Wilkinson power divider, and the divided signals are passed through each BM to select whether or not to invert 180°. After passing through the BM, the signals are transmitted to the bi-directional core, and the backward operation is the same as the forward operation, allowing for gain adjustment. Finally, when the signal is synthesized, it passes through an HC-based I, Q combiner,

where the signals are synthesized with a 90° phase delay. In Sections III and IV, we will describe the techniques for implementing the active bi-directional scheme and the design and performance of each block.

III. Bi-Directional Core Design

A. Matching Procedure Comparison for the Active Bi-Directional Operation

For the efficient design of symmetrical active bi-directional behavior, two aspects need to be verified.

1) Core structure that supports bi-directional behavior.
2) Matching performance between bi-directional behaviors.

The first aspect is whether putting the network configuration as passive or active would be crucial in supporting the bi-directional behavior. In the case of a passive network without a general amplification capability, reciprocity is established and bi-directional operation is available. On the other hand, an active structure such as a common source (CS) has an amplifying feature but exhibits different bi-directional behavior. To solve this problem, another path for the active operation should be added with the selection of the activated core. In this way, the structural differences and the implementation method of the bi-directional operation core will determine the performance of the bi-directional operation.

Second, it is necessary to analyze matching performance change during the bi-directional operation. In the case of a passive network, ideally, if it has a symmetrical structure, the IO impedances are equal. This eliminates the need for a reconfigurable matching network for forward and backward operations. On the other hand, many bi-directional active circuits have different IO impedances, each with its own matching network for prior or post blocks. This implies that they require a variable network that can change matching when the operating direction changes, which in turn increases the design area or imposes the implementation complexity and losses due to the multiple use of switches [40], [41], [42]. Therefore, the matching performance and implementation complexity of these IO matching networks are critical factors in ABPS design.

Fig. 3(a) shows the matching method of a conventional ABPS utilized in [30] and [38]. Since it performs an amplification role, the IO impedances are typically different, and if the core is structurally symmetrical for bi-directional operation, we can write

$$\begin{aligned} Z_{\text{in,Core}F} &\neq Z_{\text{out,Core}F} \\ Z_{\text{in,Core}F} &= Z_{\text{in,Core}B} \\ Z_{\text{out,Core}F} &= Z_{\text{out,Core}B} \end{aligned} \tag{1}$$

where $Z_{\text{in,Core}F}$ and $Z_{\text{out,Core}F}$ represent the IO impedances for forward operation and $Z_{\text{in,Core}B}$ and $Z_{\text{out,Core}B}$ denotes the IO impedances for backward operation. Since there is a preceding block and following blocks before and after the core, impedance matching requires

$$\begin{aligned} Z_{\text{in,MNF}} &= Z_P^* \\ Z_{\text{out,MNF}} &= Z_F^* \end{aligned} \tag{2}$$

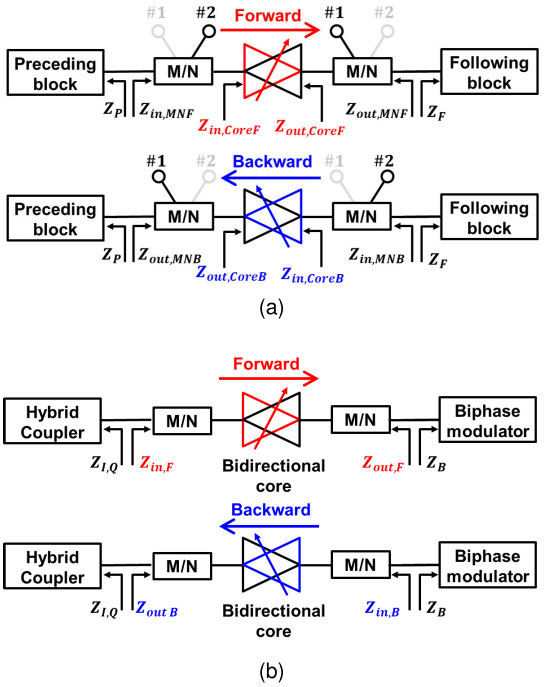

Fig. 3. Matching configuration analysis of the (a) conventional bi-directional amplifier and (b) proposed bi-directional amplifier.

in the forward direction and

$$\begin{aligned} Z_{\text{out,MNB}} &= Z_P^* \\ Z_{\text{in,MNB}} &= Z_F^* \end{aligned} \tag{3}$$

in the backward direction.

Hence, $Z_{\text{in,MNF}}$ and $Z_{\text{out,MNB}}$ must be equal for matching which can be inferred from (2), (3), which means that if you use the nonreconfigurable (i.e., passive) matching network, you will not get physically accurate impedance matching because the IO impedances are different as shown in (1). Therefore, reconfigurable matching networks are necessary to address the aforementioned issues; however, doing so increases the design area, implementation complexity, and losses due to the switch usage. In addition, the negative impacts indicated above will intensify the disparity between the impedance values of Z_P and Z_F blocks.

To solve the above-mentioned drawbacks at once, the structure shown in Fig. 3(b) is proposed, and the matching condition can be written as follows for forward operation:

$$\begin{aligned} Z_{\text{in},F} &= Z_{I,Q}^* \\ Z_{\text{out},F} &= Z_B^* \end{aligned} \tag{4}$$

where $Z_{\text{in},F}$ and $Z_{\text{out},F}$ represent the IO impedances for forward operation including the core and matching network. The other two terms $Z_{I,Q}$ and Z_B denote the input impedance of the HC and BM, respectively, and

$$\begin{aligned} Z_{\text{out},B} &= Z_{I,Q}^* \\ Z_{\text{in},B} &= Z_B^* \end{aligned} \tag{5}$$

for backward operation. If the core structure satisfies symmetry, $Z_{\text{in},F} = Z_{\text{in},B}$ and $Z_{\text{out},F} = Z_{\text{out},B}$, then applying it

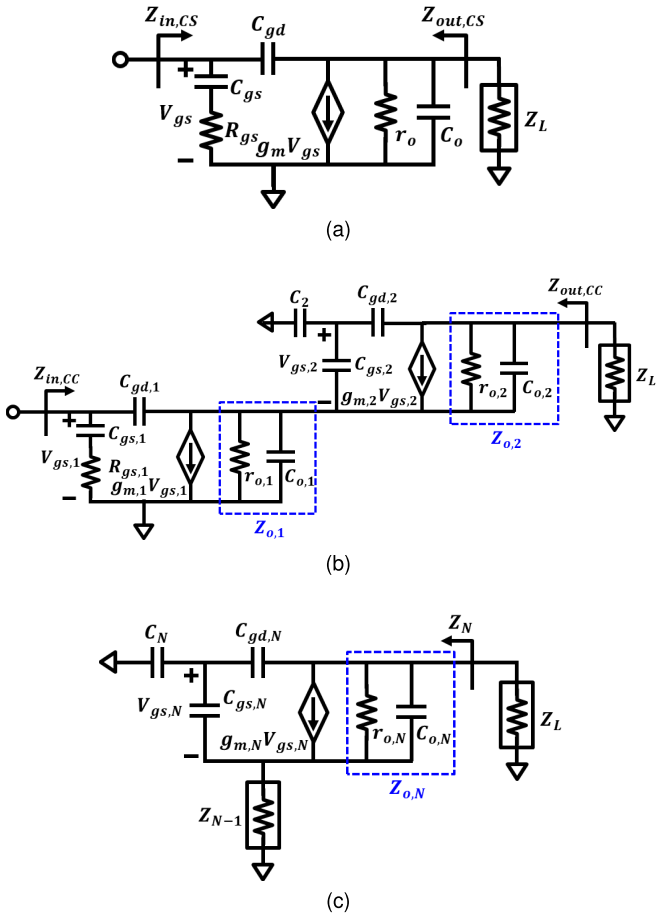

Fig. 4. Equivalent small-signal model of the different topologies. (a) CS, (b) cascode, and (c) N-stack.

to (4), (5) the IO impedances should be equalized as follows:

$$Z_{\text{in},F} = Z_{\text{out},B} = Z_{\text{in},B} = Z_{\text{out},F} = Z_{I,Q}^{*} = Z_{B}^{*}. \tag{6}$$

If this condition is satisfied, an accurate matching and symmetric operation can be achieved simultaneously at all junctions without the need for a reconfigurable matching network through additional switches.

B. Intuition of the IO Impedances Variation With the Number of Stacks

To realize the equal IO impedance described in Section III-A through a simple structure, the analysis of the IO impedance according to the amplification structure of the TR should be prioritized. As a result, in this section, we will explain the mathematical analysis and intuition of the variation of IO impedance with the number of stacks of TRs. Fig. 4 shows a small-signal equivalent model based on a general amplification structure of TRs. The IO admittances (or impedances) in the CS structure of Fig. 4(a) are expressed by the following equations:

$$Y_{\text{in,CS}} = \frac{1}{\frac{1}{sC_{\text{gs}}} + R_{\text{gs}}} + s\left[1 + g_m\left(r_o \| \frac{1}{sC_o}\right)\right]C_{\text{gd}}$$
$$Y_{\text{out,CS}} \approx \frac{1}{r_o} + s\left(C_o + C_{\text{gd}}\right). \tag{7}$$

It can be seen that the value of C_{gd} due to the Miller effect is amplified by $1 - A$, where A is the open-loop gain of the CS at the input stage. In addition, the disparity between the real part of the admittance (i.e., conductance) at the IO stage is large because of R_{gs} and r_o.

Fig. 4(b) indicates the small-signal equivalent circuit of the cascode, where C_2 is the capacitor across the gate of the second stage. Interpreting the small-signal equivalent circuit, we can get input admittance as follows:

$$Y_{\text{in,CC}} = \frac{1}{\frac{1}{sC_{\text{gs},1}} + R_{\text{gs},1}} + s(1 - A_{\text{cc}})C_{\text{gd},1}$$
$$A_{\text{cc}} = -\frac{g_{m,1}}{\left[\frac{K_2 g_{m,2} Z_{o,2} + 1}{Z_L + Z_{o,2}} + \left(\frac{1}{Z_{o,1}} + sK_2 C_{\text{gs},2}\right)\right]} \tag{8}$$

where K_2 is the effective gate capacitance factor which can be expressed as $C_2/(C_2 + C_{\text{gs},2})$. If we ignore the channel length modulation (CLM) effect, the gain can be modified into

$$A_{\text{CC}}\,|_{\text{woCLM}} = -\frac{g_{m,1}}{K_2 g_{m,2} + sK_2 C_{\text{gs},2}}. \tag{9}$$

Again, the Miller effect due to amplification is taken into account, but in reality, the conductance of the CS and cascode are almost identical, with only the susceptance being slightly different.

The important part is the analysis on the output side, and if we ignore C_{gd} and expand the equation, we can express the impedance as follows:

$$\begin{aligned} Z_{\text{out,CC}} &= \left[1 + K_2 g_{m,2}\left(r_{o,2} \| \frac{1}{sC_{o,2}}\right)\right] \\ &\quad \left[r_{o,1} \| \frac{1}{s(C_{o,1} + K_2 C_{\text{gs},2})}\right] + \left(r_{o,2} \| \frac{1}{sC_{o,2}}\right) \\ &= (1 + K_2 g_{m,2} Z_{o,2})\left[Z_{o,1} \| \frac{1}{s(K_2 C_{\text{gs},2})}\right] + Z_{o,2} \end{aligned} \tag{10}$$

where $Z_{o,1}$ and $Z_{o,2}$ are the impedance of the output network in the first and second stack TR, respectively. Similar to the expression for the output resistance of a typical analog cascode circuit, we can see that the impedance connected to the source (i.e., $Z_{o,1}$) is amplified by $1 + K_2 g_{m,2} Z_{o,2}$ and added to the intrinsic output impedance (i.e., $Z_{o,2}$). Since the first term of (10) is much larger than the second term, we can approximate it as follows, and substituting it for the admittance, we get the following expressions:

$$Z_{\text{out,CC}} \approx (1 + K_2 g_{m,2} Z_{o,2})\left[Z_{o,1} \| \frac{1}{s(K_2 C_{\text{gs},2})}\right]$$
$$Y_{\text{out,CC}} \approx \frac{Y_{o,1} + sK_2 C_{\text{gs},2}}{1 + K_2 g_{m,2} Z_{o,2}} \approx \frac{Y_{o,1} + sK_2 C_{\text{gs},2}}{1 + K_2 g_{m,2} r_{o,2}}. \tag{11}$$

Based on (11), we can expand this into an admittance for an N-stack like the one in Fig. 4(c), as given by

$$Y_N \approx \frac{Y_{N-1} + sK_N C_{\text{gs},N}}{1 + K_N g_{m,N} r_{o,N}} \tag{12}$$

where K_N can be expressed as $C_N/(C_N + C_{\text{gs},N})$. It is also important to note that the output admittance of this N-stack

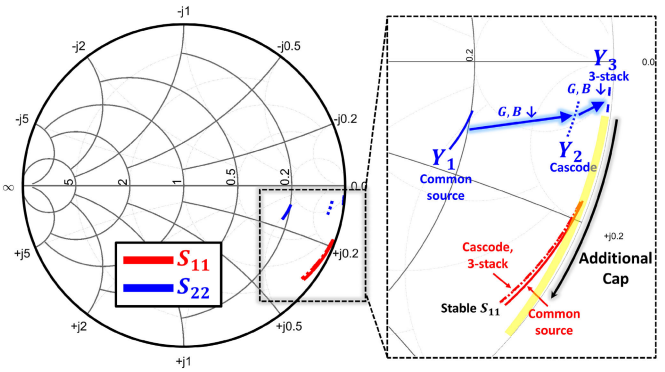

Fig. 5. Plot of the IO admittance variation with the different stack count on a Smith chart.

can be separated into real and imaginary parts, conductance and susceptance, as follows:

$$\text{Real}[Y_N] = G_N = \frac{G_{N-1}}{1 + K_N g_{m,N} r_{o,N}}$$
$$\text{Imag}[Y_N] = B_N = \frac{B_{N-1} + wK_N C_{\text{gs},N}}{1 + K_N g_{m,N} r_{o,N}}. \quad (13)$$

A closer look at (13) shows that as the number of stacks increases, the real and imaginary parts of the admittance, that is, conductance and susceptance, decrease by $1 + K_N g_{m,N} r_{o,N}$. Intuitively, the decrease in conductance implies a shift to the right on the admittance Smith chart, while the decrease in susceptance implies a counterclockwise rotation due to a decrease in total capacitance. From another perspective, K_N changes depending on the value of the capacitance attached to the TR's gate (i.e., C_N), where K_N is a value between 0 and 1, 1 for very large C_N values and 1/2 for values equal to $C_{\text{gs},N}$. As a result, we can vary the admittance not only by the number of stacks but also by the C_N value. The IO admittance trajectories, compared to the number of stacks, are plotted on the admittance Smith chart in Fig. 5. We can see that S11, which is related to input impedance (admittance), is almost insensitive to the number of stacks. In contrast, as shown in the previous equation, as the number of stacks increases, S22 moves to the right side of the Smith chart and rotates counterclockwise with a decrease in susceptance. If we adjust the number of stacks and C_N to equalize the input conductance and add an additional parallel capacitor as shown by the black arrow in Fig. 5, we can achieve the identical IO impedance without the need for an additional bulky matching network, which will be discussed in Section III-C.

C. Proposed Equivalent IO Impedances Bi-Directional Structure

Fig. 6 shows the switch-less bi-directional amplification operation structure with the same IO impedances proposed in this article, and Fig. 6(a) and (b) illustrates the forward and backward operation methods, respectively. The proposed structure combines two three-stack cores in a staggered manner for effective bi-directional operation. It is a compact structure in which the gate of one core is directly connected to the drain of another core. During forward operation, signals are transmitted

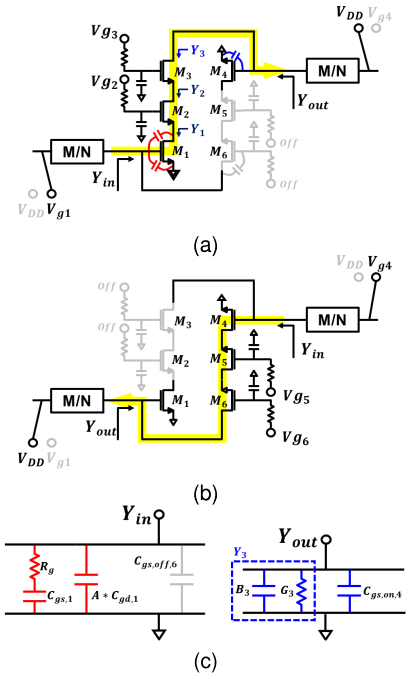

Fig. 6. Schematic of the proposed switch-less staggered architecture. (a) Forward operation, (b) backward operation, and (c) major parasitic components on the IO side under forward operation.

through M_1, M_2, and M_3, and the bias of M_5 and M_6 is turned off, resulting in a large impedance. In addition, V_{dd} is applied equally to the drain of M_3 and the gate of M_4, so M_4 always operates in an ON-state during forward operation. On the other hand, in backward operation, M_2 and M_3 are disabled and the input signal passes through M_4, M_5, and M_6. In addition, the gate of M_1 is applied to V_{dd} and is always switched on, and the drain of M_3 and the gate of M_4, which were attached to V_{dd} during forward operation, are changed to Vg_4. As described above, the proposed structure determines the direction of operation solely through bias changes, without the need for a MOSFET switch.

Fig. 6(c) shows a schematic for components that appear equivalent at the IO stage during forward operation. At the input terminal of the structure, the off capacitance of M_6 is mainly visible along with $C_{\text{gs},1}$, resistance, and $C_{\text{gd},1}$ with the Miller effect applied equivalently. At the output stage, the admittance is seen from the drain of the three-stack (i.e., Y_3) and the capacitance of M_4 (i.e., $C_{\text{gs,on},4}$) which is always on-state due to V_{dd} bias state. In Section III-B, after creating the identical conductance of IO using the number of stacks and C_N, the claim that the susceptance can also be adjusted using a parallel capacitance was very simply solved by using an on C_{gs} of the M_4 of the corresponding structure. The capacitance mainly seen in the input stage is the effect of $C_{\text{gs},1}$. The output stage compensates for the very low susceptance caused by the three-stack. It does this by using the capacitance through C_{gs} of M_4, which is the same size as C_{gs} of M_1, to achieve equal susceptance of the input stage without requiring any additional matching network.

To numerically represent the degree to which the IO impedances of the structures are equal, an impedance

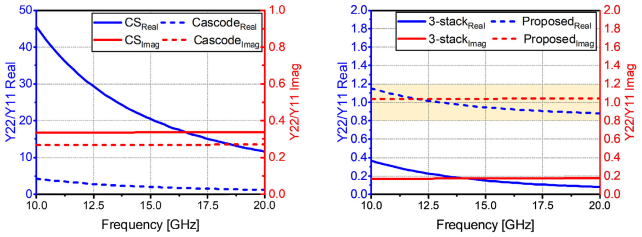

Fig. 7. IS plot utilizing the ratio of the Y11 and Y22 with (a) one- and two-stack, (b) three-stack and proposed structures.

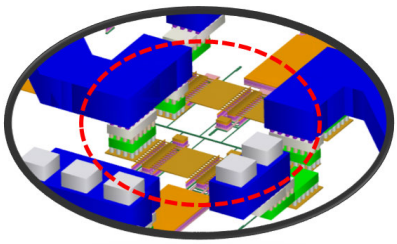

Fig. 8. EM-based layout with the proposed staggered core showing the actual connection structure.

similarity (IS) formula utilizing the Y parameter was defined, expressed as $Y22/Y11$. The closer both the real and imaginary parts of $Y22/Y11$ are to 1, the more the IO impedances are the same at that frequency. Fig. 7 shows the IS for the number of stacks and the proposed structure. The blue and red lines in Fig. 7(a) show the IS of the real and imaginary parts, respectively, and the solid and dashed lines indicate the results for the CS and cascode structures, respectively. The IS of the real part of the CS is about 50–10, indicating a severe IO imbalance, while the IS of the real part of the cascode is reduced to 5 or less. The IS of the imaginary part also decreased when changing from a CS to a cascode.

Fig. 7(b) shows the three-stack and the proposed structure, which are depicted by solid and dashed lines, respectively. We can see that both the real and imaginary parts of IS decrease from the cascode and move away from the value of 1 in three-stack, while the proposed structure is close to 1 for both real and imaginary parts. Finally, the identical IO impedance at a certain frequency was obtained with the proposed structure, and the EM effect was reflected and optimized by wiring staggered TRs as shown in Fig. 8.

IV. Full Schematic of the VABPS

Fig. 9 represents the overall schematic of the proposed VABPS. As described earlier in Fig. 2, the signal for each path is scaled in the amplification core through a transformer-based coupler that generates I and Q signals. The signal is then synthesized in the WPC through a BM that selects 0° and 180°. In Sections IV-A–IV-D, we describe the EM-based performance and structure of each block in more detail.

A. Proposed Core Structure With the Matching Network

The cores with the identical IO impedances described in Section III were matched utilizing inductors and single-ended 2-to-1 transformers. The design parameters for these components are shown in Table I. The EM-based S parameter performance of the core with the matching network is shown in Fig. 10. As shown in Fig. 10(a) and (b), S21 and S12 correspond to each other in forward and backward operation, and the gain value is found to be 11.5 dB at 16 GHz. It is also important to note that the values of S11 and S22 in forward and backward operations are almost identical to each other, indicating that the same IO matching is achieved even with the EM structure. In addition, the gain can be adjusted by varying the gate bias of the third stacked TR of each staggered core, and the result is shown in Fig. 10(c) and (d). By adjusting the bias voltage, a variable gain range of 20 dB can be achieved, with a phase shift range of less than 7°. In practice, a phase shift of 7° when varying the gain does not have a significant effect on the performance of the PS of an I and Q synthesized method such as VABPS. The reason for this is that when the I and Q paths have the same gain, they are delayed by the same amount of phase, so there is no problem in synthesizing them. In the same manner, when the I and Q paths have a large difference in gain, they suffer different phase delays, but since the gain of one path is small, the effective phase value that is actually distorted when the I and Q signals are combined is relatively small.

B. Miniaturized Transformer-Based HC

Key performance metrics for I and Q signal generators include loss, bandwidth, size, and IS between I and Q ports. Moreover, many different structures generate the I and Q signals, which are most important in VSPS designs, including RC-PPF, Lange couplers, quadrature all-pass filters (QAFs), and HC. PPFs can be implemented in a small size but are known to have very high losses, and Lange couplers are branch line length-based structures with the disadvantage of having a large layout. In addition, QAFs have the advantage of moderate design area and loss, but the bandwidth is limited by the load capacitance. Therefore, transformer-based HCs have been used and studied as quadrature generators in various articles in recent years because of their moderate size and loss with adequate bandwidth. Most of them utilize the vertical coupling method with an enhanced coupling coefficient to improve the performance of the quadrature generator, but in this article, the enhanced lateral symmetric coupling method is applied to improve the IS between the ports that generate the I and Q signals.

Fig. 11 depicts a layout and the equivalent circuit of the transformer-based HC, which has four terminals: an isolation (ISO), a coupling (CPL), an input (IN), and a through (THRU). Every component is made up of a coupled transformer, in which the coupling factor is denoted by k_L, the self-inductance by L, the capacitor between the primary and secondary turns by C_c, and the ground by C_g. According to the odd–even mode analysis [29], the model parameter of the

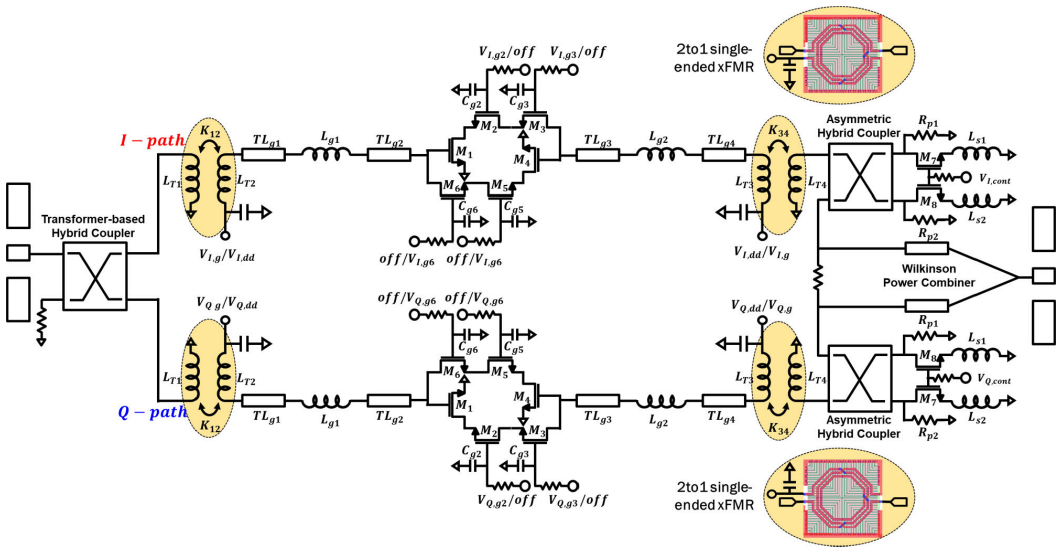

Fig. 9. Full schematic of the proposed VABPS.

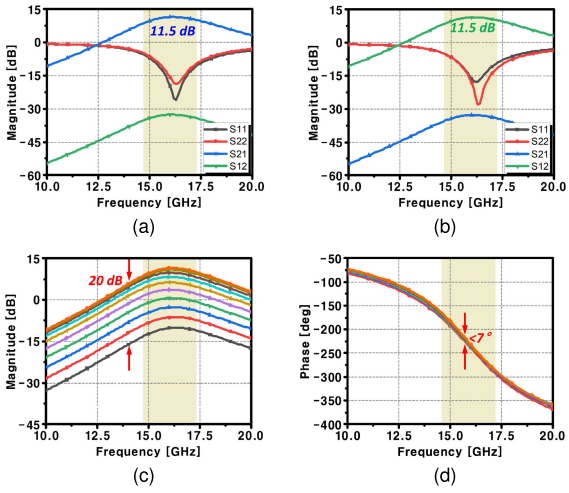

Fig. 10. EM simulated S parameter results on (a) forward, (b) backward path, (c) forward path magnitude under the gain variation, and (d) phase under the gain variation.

TABLE I

DESIGN PARAMETERS OF THE VABPS

$L_{T1,4}$ 172 pH	$L_{T2,3}$ 530 pH	$K_{12,34}$ 0.67	$L_{g1,2}$ 128 pH
$TL_{g1\sim4}$ 55 Ω, 100um	$C_{g2,3,5,6}$ 100 fF	$(W/L)_{1\sim6}$ 25 um / 90 nm	$(W/L)_{7,8}$ 120 um / 28 nm
$L_{s1,2}$ 65 pH	$R_{p1,2}$ 1.1 KΩ		

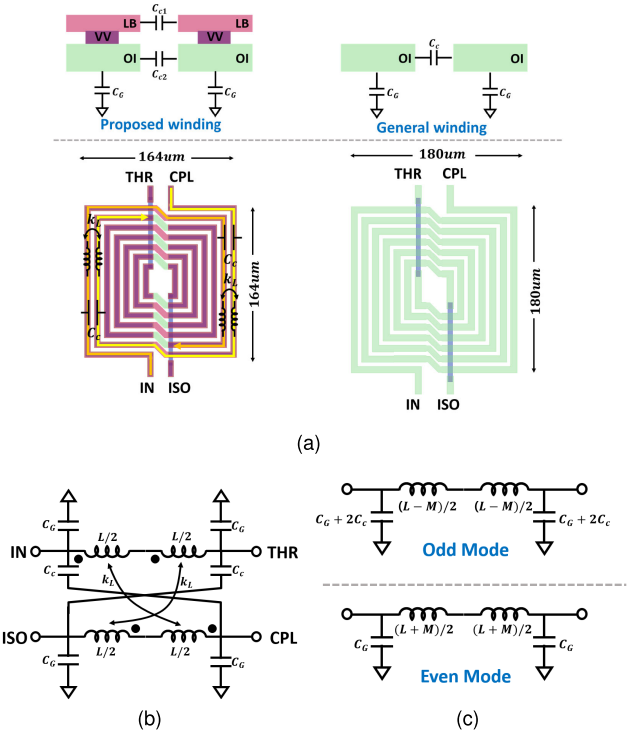

Fig. 11. (a) EM model of a proposed and conventional transformer-based HC, (b) equivalent circuit model of the coupler, and (c) even and odd half-circuit model of the coupler.

HC can be derived as follows:

$$L = \frac{Z_o}{w_o\sqrt{1-k_L^2}}$$
$$C = \frac{1}{Z_o w_o\sqrt{1-k_L^2}}$$
$$C_G = C(1-k_L)$$
$$C_c = Ck_L \quad (14)$$

where w_o is the coupling frequency. Not limited to the formula above, many articles [16], [29], [43] have used the case with a coupling coefficient of $k_L = 0.707$ or higher because of the bandwidth enhancement and the reduction of the design area. Fundamentally, lateral coupling has an upper limit, and vertical coupling is widely used to increase the coupling coefficient accordingly. However, to use vertical coupling in a typical CMOS process, different layers of metal must be utilized. This, in turn, leads to impedance differences between the CPL and THR ports, which generate I and Q signals. Since the CPL and THR ports are directly connected to the active bi-directional core, more accurate impedance matching is required.

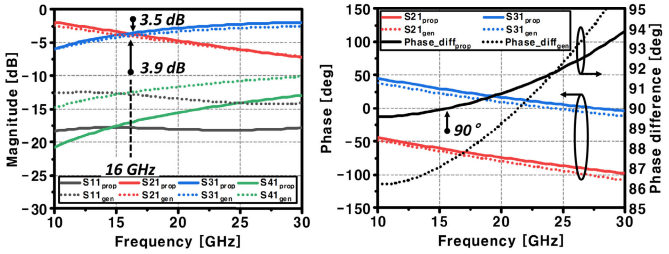

Fig. 12. S parameter results of the EM simulated transformer-based HC. (a) Magnitude response and (b) phase response.

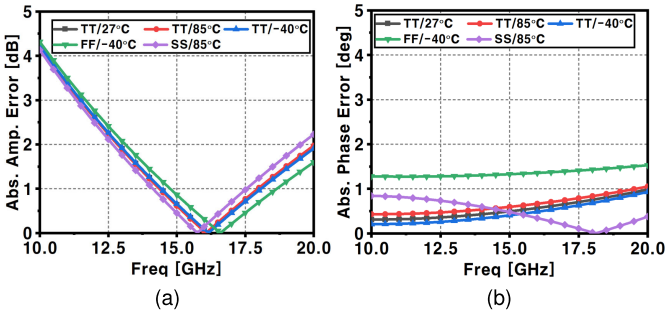

Fig. 13. EM simulated absolute amplitude and phase errors of transformer-based HC under process corner and temperature variations. (a) Amplitude error and (b) phase error.

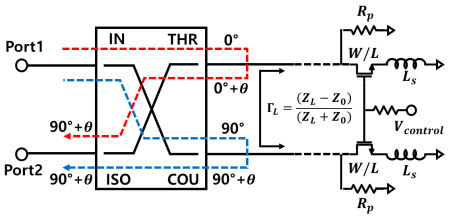

Fig. 14. Schematic of BM with reflective load.

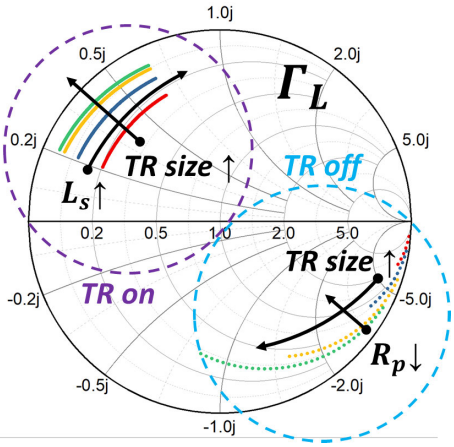

Fig. 15. Reflection coefficient trajectory of a reflective load on a Smith chart as a function of design parameter variation.

Therefore, the proposed circuit employs lateral coupling with transformer structure as shown in the left side of Fig. 11(a). Including the general winding, both couplers are designed to operate at 16 GHz and have a single side length of 164 μm for the proposed winding and 180 μm for the general winding. In the case of the proposed method, each of the two coupled lines is composed of the same metal with LB-VV-OI connected and has 3.5 winding turns to reduce the chip size. The general design of a coupler, most of them utilizes one metal (i.e., OI). Still, two metals (i.e., LB-VV-OI) are tied together to obtain additional coupling capacitance (i.e., $C_{c1,c2}$) and increase the quality factor of the inductor while maintaining C_p due to the ground.

The EM-based S-parameter results of the HC with the different winding methods are compared in Fig. 12. As shown in Fig. 12(a), the general one-metal winding exhibits a loss of 3.9 dB, while the proposed scheme has a loss of 3.5 dB at around 16 GHz. The proposed method exhibits lower losses in a smaller design area than the conventional method, which can be attributed to the decrease in w_o due to the inclusion of C_c and the slight rise in mutual inductance. Matching performance such as S11 and S41 are also better. Furthermore, both winding schemes utilize an identical metal layer, so each port has a very high matching similarity. Fig. 12(b) shows that the proposed scheme also has better characteristics in terms of the phase difference of I and Q signals. The proposed winding has a phase difference of about 90° in the 16 GHz, and a comparison of the phase difference from 10 to 30 GHz shows a more moderate slope. As a result, it is possible to design the HC with a miniaturized area without adding other devices while ensuring the matching uniformity of all ports. Fig. 13 shows the absolute errors in amplitude and phase between ports 2 and 3 in the corner simulation of the proposed HC. Since port 4 of the HC is terminated with a 50-Ω resistor, there is a slight mismatch due to process and temperature changes, but since it is a line-based I and Q generator, it can be seen that the variations are very small.

C. BM Design With the Nonideal Coupler

Since the generation of I and Q signals alone cannot achieve a full 360° phase range, it necessitates the inclusion of a block capable of implementing a 180° phase inversion for each I and Q signal. Although a 180° phase inversion is straightforwardly realized by reversing the connections in a differential structure, the proposed circuit must employ an alternative approach due to its single-ended operation. In this configuration, the BM [6], [23], [44] with a reflection method is utilized for 180° phase delay, as depicted in Fig. 14. The signal fed into port 1 of the HC is reflected from the THR and CPL ports and then coherently combined at port 2. Compared to a different design that utilizes a low-pass filter (LPF) and high-pass filter (HPF) instead of the coupler, such a BM inherently offers a broader operating bandwidth [6] and minimal impedance variation during phase transitions.

The BM illustrated in Fig. 14 comprises an HC and a reflective load, where the reflective load consists of a TR, an inductance (L_s) directly connected to ground, and a parallel resistance (R_p), which are toggled based on the applied bias voltage. The BM must exhibit low and equal insertion loss in both the TR on and off states, while also maintaining a reliable 180° phase difference. The magnitude and phase of the reflection coefficient (i.e., Γ_L) as a function of the voltage dictate the BM's performance. The reflection coefficient's trajectory on a Smith chart, influenced by design parameters, is shown in Fig. 15. As the TR size increases,

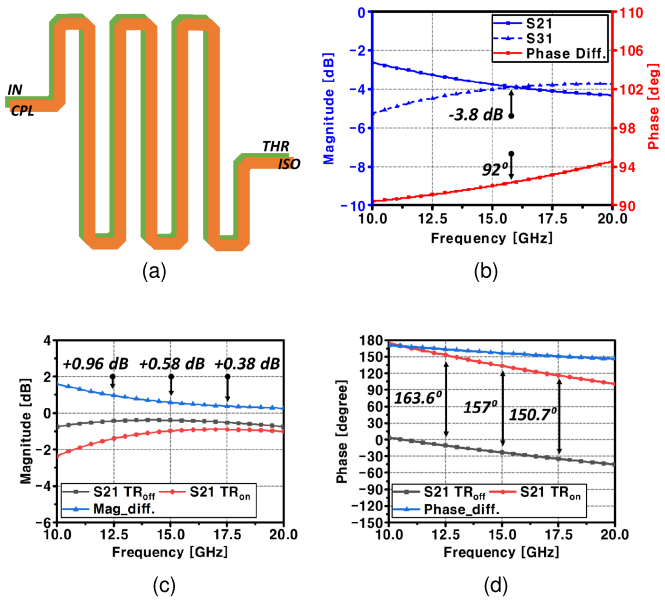

Fig. 16. Typical coupled line-based HC with a (a) layout and (b) S parameter magnitude response with IQ phase difference. S parameter results of the BM with nonideal HC and ideal load. (c) Magnitude response and (d) phase response.

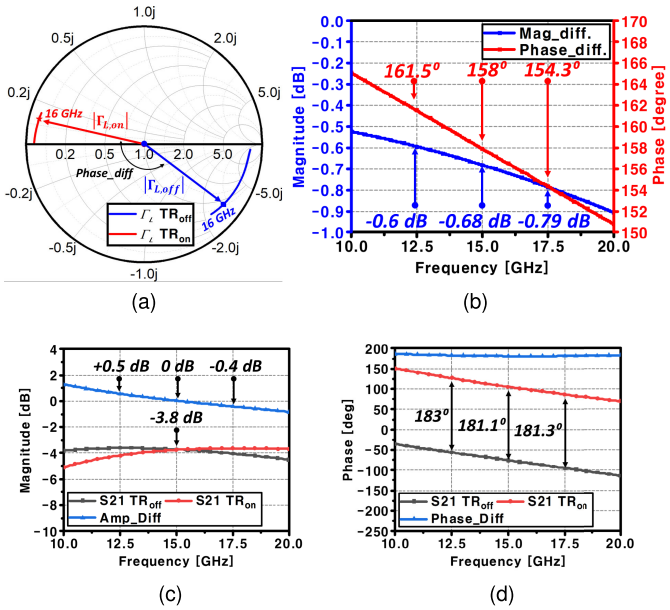

Fig. 17. (a) Smith chart trajectory, (b) magnitude and phase differences of the optimal reflective load's reflection coefficient and EM-based S parameter results of the proposed BM with the optimal reflective load. (c) Magnitude response and (d) phase response.

its on-resistance decreases, enhancing the magnitude of the reflection coefficient; however, the parasitic capacitance of a larger TR also increases, affecting the reactance. The 180° phase shift distortion introduced by the TR's parasitic capacitance can be compensated by incorporating L_s, while discrepancies in the reflection coefficient magnitude between on and off states can be mitigated by adjusting R_p. Thus, by optimizing these design parameters, a reflection coefficient with consistent magnitude and a 180° phase difference can be achieved [44].

However, even if the HC employed in the BM design achieves an equal magnitude response with a 90° phase difference between the CPL and THR ports at the operating frequency, performance degradation can occur due to the inherent limitations of the HC's quality factor and coupling coefficient [45]. In [45] and [16], the impact of a nonideal HC on the performance of an RTPS was analyzed using (15), as shown in the equation at the bottom of the page, revealing that lower quality factors and coupling coefficients exacerbate insertion loss variations at the 180° phase transition. For instance, the coupled line coupler depicted in Fig. 16(a) demonstrates S21 and S31 of 3.8 dB with a 92° phase difference at 16 GHz. However, performance degradation is observed when connected with an ideal load (i.e., $\Gamma_L = e^{j\theta}, e^{j(\theta+\pi)}$). Specifically, Fig. 16(c) and (d) illustrates the combination of a nonideal HC with an ideal load, showing a 0.58 dB difference in S21 when the TR is toggled, and a phase discrepancy of 157° instead of 180° at 15 GHz, underscoring the performance degradation even under ideal loading conditions. Consequently, the HC and reflective load co-design process is crucial for effective BM design.

To design an optimal BM, it is necessary to analyze the effect of nonideal HC and the characteristics of the reflected load. For example, in the ideal case, the reflection coefficients of the phase transition state and the original state should be the same in magnitude and exactly 180° apart in phase. However, the reflected load should intentionally create a magnitude difference and phase offset to account for the change in insertion loss of the actual HC. In simpler terms, Fig. 16(c) shows that the RTPS with a nonideal coupler has a larger insertion loss when the TR is on than when it is off, so the actual reflective load should have a larger magnitude of the reflection coefficient when the TR is on.

Fig. 17 presents the Smith chart of the reflection coefficient as a function of the frequency of the optimal reflective load used in the proposed BM, and the magnitude and phase difference of the TR ON–OFF state with the final performance of the proposed BM. As seen in Fig. 17(a), the reflection coefficient in the 16-GHz band actually has a larger magnitude when the TR is on than when it is off, and the phase difference is not 180°. In fact, at 15 GHz, the optimal load on the HC for this structure results in a 0.68 dB difference in reflection coefficient magnitude and a 158° phase difference as shown

$$S_{21ps} = S_{41C} + \frac{2S_{21C}S_{31C}\Gamma_L - 2S_{11C}S_{21C}S_{31C}\Gamma_L^2 + S_{41C}\left(S_{21C}^2 + S_{31C}^2\right)\Gamma_L^2}{1 - 2S_{11C}\Gamma_L + S_{11C}^2\Gamma_L^2 - S_{41C}^2\Gamma_L^2} \tag{15}$$

$$S_{11ps} = S_{11C} + \frac{\left(S_{21C}^2 + S_{31C}^2\right)\Gamma_L - S_{11C}\left(S_{21C}^2 + S_{31C}^2\right)\Gamma_L^2 + 2S_{21C}S_{31C}S_{41C}\Gamma_L^2}{1 - 2S_{11C}\Gamma_L + S_{11C}^2\Gamma_L^2 - S_{41C}^2\Gamma_L^2} \tag{16}$$

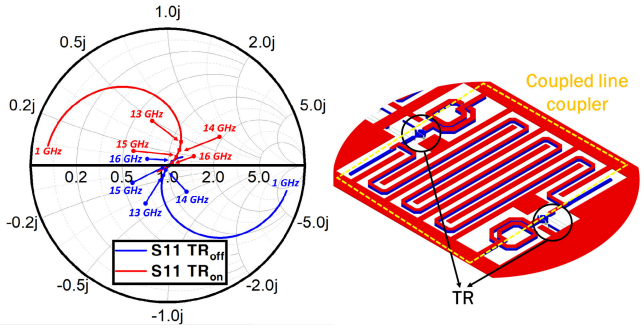

Fig. 18. (a) Input impedance variation under phase transition state and (b) three-dimensional EM structure of the proposed BM.

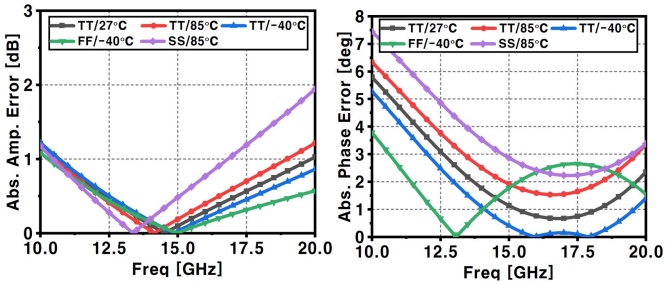

Fig. 19. EM simulated absolute amplitude and phase errors of BM under process corner and temperature variations. (a) Amplitude error and (b) phase error.

in Fig. 17(b). The final EM-based performance of the BM with these optimal loads and HCs is shown in Fig. 17(c) and (d). It has an insertion loss of −3.8 dB at 15 GHz, with differences within 0.5 dB at 12.5 and 17.5 GHz, and a phase difference of 181° to 183° at those frequencies, indicating that it can perform accurate phase inversion at the center frequency.

As an advantage of BM, it can operate over a wider bandwidth than LPF and HPF type, in general, and also has a great advantage in terms of matching uniformity by utilizing symmetry. Even if the magnitude and phase of S21 at 180° phase inversion are accurate in BM operation, the input impedance must be nearly uniform to maintain the uniform performance of the blocks in front and behind, which in turn determines the performance of the entire block. Therefore, BM using HC exhibits regularity between the phase inversion behavior of the input impedance when a reflective load is combined due to its intrinsic structural symmetry. Fig. 18 shows the input matching performance of the EM-based BM and the designed EM 3-D layout. As illustrated in Fig. 18(a), it can be observed that the trajectories of S11 with TR on and off are almost symmetrical, and in fact, the input impedance exists at almost the same location in the 16 GHz. This allows us to maintain an invariant impedance during the ON–OFF state transition, which improves the reliability of the prior and postblock behavior.

Fig. 19 shows the absolute amplitude and phase mismatch results for the 0° and 180° phase transition states as a function of process corner and temperature for the designed BM. Since BMs are composed of resistors and MOSFETs, they are

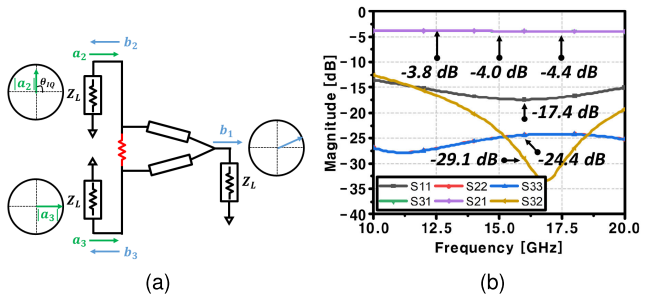

Fig. 20. (a) Schematic and (b) EM-based S parameter results of the WPC.

relatively more sensitive to process and temperature changes than HC. Similar to the previous results, it shows a very low mismatch at TT and 27 °C conditions, but up to 3° phase error at the center frequency in the corner simulation.

D. Wilkinson Power Combiner With Impedance Mismatch Mitigation

In the proposed VABPS, the gain-adjusted I and Q signals at the core are synthesized by the BM after selecting phase inversion of 0° and 180°, which can cover a phase range of 360°. A WPC eliminates the impedance mismatch when synthesizing the ±I and Q signals after passing through the BM. Fig. 20 shows the schematic of a general WPC. Assuming that a_2 and a_3 are the input I and Q signals, which can be defined as

$$\frac{a_2}{a_3} = \frac{|a_2|}{|a_3|} e^{j\theta_{I,Q}} = \gamma e^{j\theta_{I,Q}} \tag{17}$$

where $\theta_{I,Q}$ denotes the phase difference of I and Q signals. If the PC is ideal, the reflected voltage wave at that time can be expressed as follows according to [31]:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 0 & -j/\sqrt{2} & -j/\sqrt{2} \\ -j/\sqrt{2} & 0 & 0 \\ -j/\sqrt{2} & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 \\ a_2 \\ a_3 \end{bmatrix} \tag{18}$$

$$= \begin{bmatrix} -j(a_2+a_3)/\sqrt{2} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -ja_3(\gamma e^{j\theta_{I,Q}}+1)/\sqrt{2} \\ 0 \\ 0 \end{bmatrix}. \tag{19}$$

The input power is $|a_2|^2 + |a_3|^2$, and the power at the output is equal to $|b_1|^2$, so the synthesis gain can be written as

$$G_c = 10\log\frac{|b_1|^2}{|a_2|^2+|a_3|^2} = 10\log\frac{|1+\gamma e^{j\theta_{I,Q}}|}{1+\gamma^2} - 3. \tag{20}$$

As a result, we can see that the synthesis of a quadrature signal, rather than the synthesis of a typical in-phase signal on a WPC, inherently introduces a loss of 3 dB, and no matter what combination of I and Q signal phases and magnitudes are applied, there is still no reflected wave to the input port. This increases the matching efficiency by preventing reflected waves to the previous block, the BM. Moreover, since the output ports of each BM are matched by 50 Ω, it becomes a more efficient signal synthesis method than the current combining method. The EM-based S parameter results of the WPC used in the actual VABPS are shown in Fig. 20(b), and

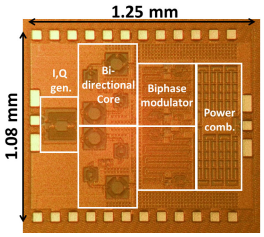

Fig. 21. Chip micrograph of the proposed VABPS. (Core area = 1.25 × 1.08 mm.)

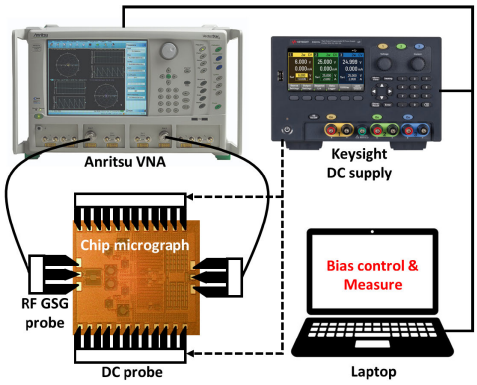

Fig. 22. Block diagram illustration of the chip measurement setup. (Core area = 1.25 × 1.08 mm.)

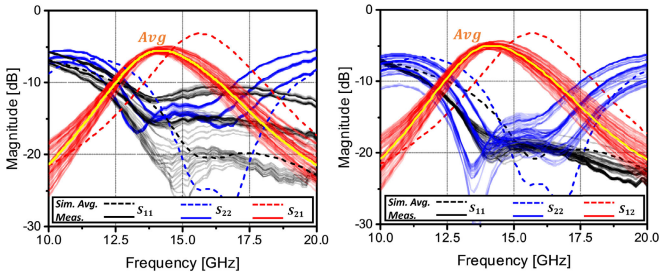

Fig. 23. Measured S parameter of the proposed PS under (a) forward operation and (b) backward operation.

it can be found that they have equal S21 and S31 values of 4 dB at 15 GHz.

V. Measurement Results

To validate the concept, a prototype based on the proposed architecture was fabricated and evaluated using a commercial 28-nm bulk CMOS process. Fig. 21 presents the die micrograph of the proposed VABPS, with a core chip area measuring 1.25 × 1.08 mm^2. Fig. 22 shows the block diagram of the measurement system of the proposed circuit. The S parameter measurements were performed with a two-port Anritsu MS4647 VNA, and the bias to drive the phase shift operation was applied with an E36200 from Keysight. After applying the desired dc bias by simultaneously connecting the dc supply, VNA, and laptop, the measured S parameter was stored.

The measured input, output return losses, and S21 for the 64 phase states under forward and backward operation are illustrated in Fig. 23(a) and (b). It is observed that the measured output return loss (S22) is less than −10 dB across the 12.5 GHz to over 20-GHz band for all states under both operation directions. However, the bandwidth for the input return loss (S11) is narrower, spanning 4.5 GHz from 12.5 to 17 GHz. For both operating states, matching was achieved normally for all phase transition states, but it can be seen that the S parameter deviation is larger for the forward S11 [black line in Fig. 23(a)]. This can be seen as a calibration error caused by the instability of the probe's pad contact due to the time taken between various bias sweeps, and the deviation was reduced by remeasuring in backward operation.

For the transmission coefficient (S21), it can be seen that the average gain is almost identical for both operating directions, with a gain of about −5.4 dB at 14 GHz. It can also be seen that S21 at 13 GHz is 1–2 dB smaller than at 14 or 15 GHz. This imbalance may have some impact on the signal integrity, but in the relatively small bandwidth used in the upper-mid band, it does not have a significant effect on the group delay distortion and can be compensated by frequency selective processing when sufficient SNR is available.

The full EM-based simulation shows −3.14 and −3.23 dB at 15.5 GHz, indicating a gain reduction of about 2 dB and a downward frequency shift. This can be attributed to some reasons: first, the single-ended operation requires an accurate ac ground to be formed where dc is applied in the core I/O matching network in a 2-to-1 transformer block. However, the ac ground is not accurately formed due to chip-wide ground instability, resulting in a longer electrical length. This resulted in a decrease in operating frequency, a shift in the matching point, and a decrease in gain; second, the parasitic capacitance on the TR routing of the staggered core, which is responsible for the amplification function in the simulation, is not accurately reflected in the simulation, so it is interpreted as having a smaller capacitance, and the center frequency is thought to have changed in the actual measurement. However, due to the wide operating bandwidth of the other blocks (such as maintaining the phase difference of I and Q signals and the operating bandwidth of BM), it was possible to show high performance not only in terms of gain but also in terms of rms errors at 14 GHz.

As shown in Fig. 24(a) and (b), the phase shift operation of the chosen 6-bit state can cover 360° in a step of 5.6°. Moreover, the polar plot on the respective frequency is presented in Fig. 24(c) to (h) representing the similar circuit behavior between forward and backward operation. Furthermore, a new metric needs to be defined and compared to indicate the uniformity of the forward and backward operation. The consistency of the magnitude response and phase response of forward and backward operation allows us to define gain consistency (GC) and phase consistency (PC) as follows, which are comparisons of the same state (with only the direction of motion reversed):

$$\mathrm{PC} = \Delta\Phi = \sqrt{\frac{1}{2^N}\sum_{i=1}^{2^N} |\Phi_{i,\mathrm{forward}} - \Phi_{i,\mathrm{backward}}|^2} \qquad (21)$$

$$\mathrm{GC} = \Delta A = \sqrt{\frac{1}{2^N}\sum_{i=1}^{2^N} |A_{i,\mathrm{forward}} - A_{i,\mathrm{backward}}|^2} \qquad (22)$$

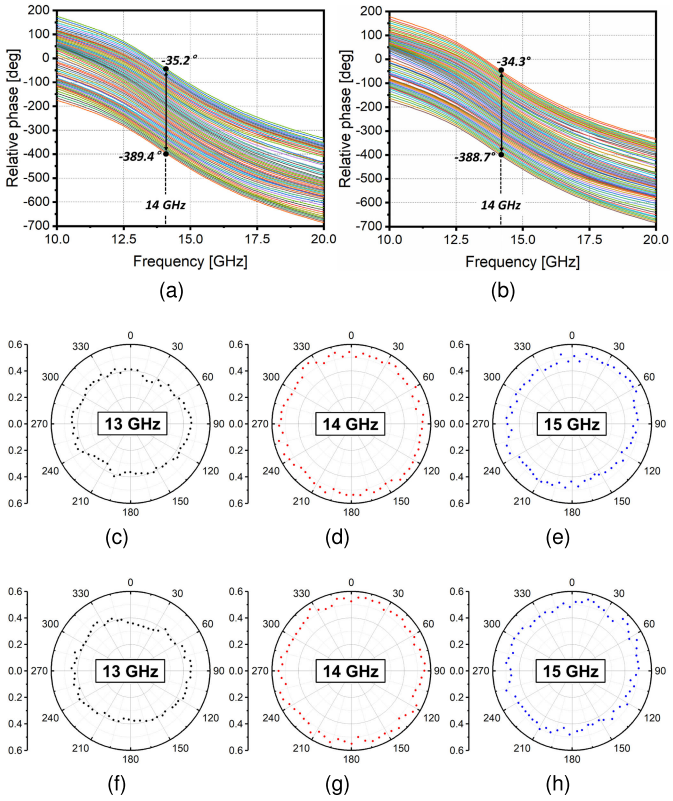

Fig. 24. Measured phase response versus frequency of VABPS under (a) forward operation and (b) backward operation and polar plot under forward operation at (c) 13 GHz, (d) 14 GHz, (e) 15 GHz and backward operation at (f) 13 GHz, (g) 14 GHz and (h) 15 GHz.

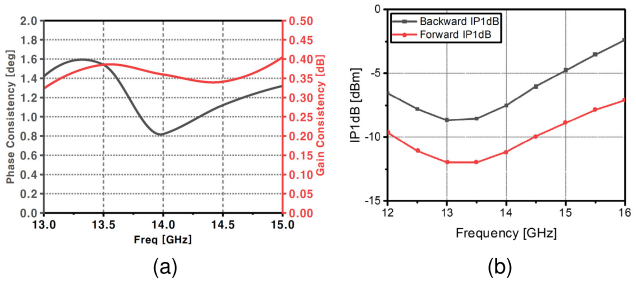

Fig. 25. (a) Measured gain and phase consistency under bi-directional operation and (b) measured input 1-dB compression point with frequencies.

where N is the number of bits and n is the respective phase state. Fig. 25(a) exhibits the gain and PC under bi-directional operation calculated by (21) and (22). At the center frequency of 14 GHz, the 64-phase shift states revealed an average phase difference of 0.8° between the forward and backward behavior and a gain difference of 0.36 dB, confirming the nearly similar bi-directional behavior. Fig. 25(b) shows the measured input 1-dB compression points, showing the lowest input levels from 13 to 14 GHz. IP1dB of −11.9 dBm in the forward direction and IP1dB of −8.5 dBm in the backward direction were measured, indicating different linearity performance. The reason for this is that in backward operation, the signal is injected into the core through the PC and BM, while in forward operation, the signal is applied directly to the core through the HC. The small amount of loss before the amplifier stage in forward operation inevitably leads to lower linearity in the forward direction.

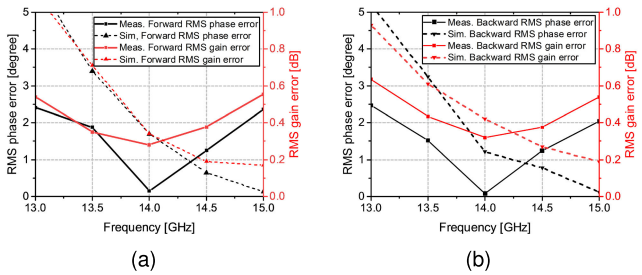

Fig. 26. Measured and simulated rms phase error and rms amplitude error under (a) forward operation and (b) backward operation.

The rms amplitude and phase errors are indicated in Fig. 26. The simulation-based rms amplitude error was found to be 0.13 and 0.19 dB with minimum values in the 15-GHz band for forward and backward operation, respectively, and 0.17° and 0.12° for phase error, respectively. On the other hand, for the measurement, the frequency with the minimum rms error was downshifted to the 14-GHz band for the aforementioned reasons, with an amplitude error of 0.28 dB with 0.16° phase error in the forward direction and 0.32 dB and 0.09° in the backward direction. From 13 to 15 GHz, we can see that both forward and backward operations have rms phase error of about 2.4° or less and amplitude error of 0.55 dB or less.

Table II provides a summary and comparison of the PS's performance with other cutting-edge efforts [25], [26], [27], [28], [29], [30], [37], [38], [39]. For comparison on the same basis with other PSs, FoMA was calculated by defining it as follows:

$$\text{FoMA} = 10\log\frac{\text{BW}(\%)\times\text{Res. bits}}{\text{rms G.E(dB)}^2\times\text{rms P.E}(^\circ)^2\times\text{Core size}_{\text{eff}}} \tag{23}$$

$$\text{Core size}_{\text{eff}} = \text{Area(mm}\times\text{mm)}/\lambda_c^2\times\text{Size factor} \tag{24}$$

where the G.E and P.E are the gain error and phase error, respectively, and the size factor is the weighting factor for PS topology. For a fair comparison with passive PSs, dc power, and S21 are excluded from the comparison. Moreover, the rms error, which is important for PS implementations, is squared so that it can be calculated as −20 log. Moreover, a larger FoMA indicates higher performance.

Since the proposed VABPS supports both active function and bi-directional operation, the chip area should be calculated relative to it. PVSPS has the advantage of bi-directional phase-shifting operation, but its losses are very high, so it requires an additional amplifier layout that can support the full operating bandwidth of the passive phase-shifter to compensate. Furthermore, if the amplifier is uni-directional, it requires twice the chip size for bi-directional operation. This results in the consumption of two types of area: passive PS + uni-directional amplifier x 2. Therefore, the size factor of the PVSPS is 3. AVSPS has somewhat lower losses but only allows uni-directional operation, so another PS is required for TRx operation. Correspondingly, the area for bi-directional operation can be thought of as being doubled. Therefore, the size factor of AVSPS is 2. Finally, active and bi-directional

TABLE II
PERFORMANCE COMPARISON WITH OTHER PSs

Ref.	IMS'23 [25]	TCAS2'21 [26]	TCAS1'22 [27]	TMTT'20 [28]	MWCL'23 [37]	TCAS1'23 [29]	ICMMT'21 [38]	RFIC'17 [39]	JSSC'20 [30]	**This work**
Technology	40 nm CMOS	130 nm CMOS	65 nm CMOS	45 nm CMOS	130 nm CMOS	130 nm SiGe	55 nm CMOS	130 nm SiGe	65 nm CMOS	**28 nm CMOS**
Bi-directional Available	O	O	O	X	X	X	O	O	O	O
Topology	PVSPS	PVSPS	PVSPS	AVSPS	AVSPS	AVSPS	Switch +AVSPS	ASTPS	Switch +AVSPS	**Switch-less+AVSPS**
Frequency (GHz)	26-32	28-38	23-40	22-44	8-12	18-30	14-18	8-12	26.5-29.5	**13-15**
Resolution (bits)	6	6	7	5	6	6	6	6	6	**6**
Peak Average Gain (dB)	-19	-10	-17.1	-7.5[1)]	-3.1∼-0.8	1.1	-4∼-1[2)]	>11.5	0	**-5.4**
RMS Gain Error (dB)	<1.2	<0.6	<0.36	<1.6	<0.24	<1.4	0.5[2)]	<0.9	<0.4	$<$ **0.55**
RMS Phase Error (°)	<2.6	3	<1.6	<3	<0.29	<3.4	2.6[2)]	<2.2	<2	$<$ **2.4**
Input P_{1dB} (dBm)	14	N/A	10.2∼13.5	-4∼1.5	8.5	-1	N/A	-15	-9.6[3)]	**-11.9/-8.5[4)]**
DC Power (mW)	0	0	0	62	90	12.2	33.6	195	20	**15.8**
Core Chip Size (mm^2)	0.63x0.24	0.5x0.3	0.63x0.24	0.9x0.7[1)]	1.7x0.54	0.99x0.28	0.95x0.5	2.6x1.5	0.6x0.5[1)]	**1.25x1.08**[5)]
Core size factor	3	3	3	2	2	2	1	1	1	1
FoMA[6)]	34.8	33.7	33.9	29.2	37.9	35.6	39.7[2)]	34.7	36.9	36.4

[1)] Estimated from figures; [2)] Simulated results; [3)] -9.6 dB addition from IIP3; [4)] Forward and backward operation;
[5)] Including pads
[6)] FoMA = $10log(BW(\%) \times Res.\ bits) - 20log(RMS\ gain\ error \times RMS\ phase\ error) - 10log(Core\ size_{eff})$
PVSPS: Passive vector sum PS; AVSPS: Active vector sum PS; ASTPS: Active switch type PS

available PS satisfies the bi-directional operation and amplifier in a single chip, therefore, the size factor is only 1.

The FoMA is then calculated as shown in Table II, proposed VABPS ranks fourth out of the ten comparisons. It can be seen that the proposed switch-less AVSPS may be large when compared to the physical size, but it shows relatively high performance when applying FoMA considering that it supports bi-directional behavior and includes an amplification structure. Compared with existing ABPS [30], [38], [39], the proposed VABPS achieves bi-directional operation without reconfigurable networks and switches by utilizing the intrinsic characteristics and routing of TRs, and has low rms errors.

VI. CONCLUSION

This article introduces a VABPS designed for Ku-band operation, featuring low rms gain and phase errors along with low power consumption. Traditional amplification architectures address the variability in IO impedances during bi-directional operation by incorporating a reconfigurable matching network. In contrast, this work presents an equivalent IO matching technique that obviates the need for an additional variable matching network. To achieve this, a three-stack, switch-less staggered structure is proposed, which facilitates identical IO matching. This innovation significantly enhances the reliability of bi-directional phase-shifting operations by minimizing both gain and phase errors. A transformer-based HC is employed to generate precise I and Q signals, which are fed into a BM to achieve 180° phase inversion of the I and Q signals. The proposed VABPS supports a 6-bit resolution with a phase shift range of 360° and demonstrates an rms phase error of less than 2.4° and a gain error of less than 0.55 dB, representing -5.4 dB average gain within the 13–15-GHz frequency range. The power consumption of the VABPS is approximately 15.8 mW. The chip is fabricated using a standard 28-nm CMOS process, with the core area, including the pads, 1.25×1.08 mm^2. The proposed circuit and IO impedance matching methodology are expected to be widely applicable to the design of bi-directional PSs in other frequency bands.

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