

# Low-Power Consumption and Beam-Sustainable Reconfigurable Intelligent Surface for Fixed Wireless Communication at Millimeter-Wave 5G Band

Hogyeom Kim<sup>1</sup>, Member, IEEE, Seongwoog Oh<sup>1</sup>, Member, IEEE, Manseok Kim, Member, IEEE, Byeongju Moon<sup>1</sup>, Graduate Student Member, IEEE, Jeongtaek Oh<sup>1</sup>, Student Member, IEEE, Seungwoo Bang<sup>1</sup>, Graduate Student Member, IEEE, and Jungsuek Oh<sup>1</sup>, Senior Member, IEEE

**Abstract**—This article presents a low-power consumption and beam-holding reconfigurable intelligent surface (RIS) for reliable millimeter-wave 5G fixed wireless communication. Conventional RIS designs require continuous power to maintain beamforming, with power consumption divided into two main parts: power drawn by the control board and power dissipated by unit cells. The strategies for reducing power consumption differ based on the adjustable components used. In this study, a liquid crystal (LC)-based RIS is employed to achieve low-power consumption, alongside a customized bias circuit that incorporates switches and capacitors. The proposed circuit operates using bias pulses, allowing charges to be stored in the capacitors, which in turn ensures beam sustainability. Prior research on LC-RIS reported the need for continuous power consumption and complex bias nodes to control the LC. Moreover, the proposed RIS, consisting of an  $N \times N$  array, requires only  $2N$  bias nodes for 2-D beamforming, unlike traditional RIS designs. This innovative biasing approach, referred to as an active-matrix scheme, enables a low-power, beam-sustainable RIS architecture and can be effectively applied to electrically large RIS arrays with 2-D beamforming capabilities.

**Index Terms**—Beam-sustaining, bias nodes reduction, liquid crystal (LC), low-power consumption, millimeter-wave 5G, reconfigurable intelligent surface (RIS).

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Hogyeom Kim, Byeongju Moon, Jeongtaek Oh, Seungwoo Bang, and Jungsuek Oh are with the Institute of New Media and Communication (INMC) and the Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, South Korea (e-mail: ghrua2424@snu.ac.kr; bjmoon5843@snu.ac.kr; iwalfie@snu.ac.kr; littlebang97@snu.ac.kr; jungsuek@snu.ac.kr).

Seongwoog Oh is with the School of Electrical and Computer Engineering, University of Seoul, Seoul 02504, South Korea (e-mail: ohseongwoo@uos.ac.kr).

Manseok Kim is with the Technology Research Center, ATsRO Company, Seongnam-si, Gyeonggi-do 13632, South Korea (e-mail: rnd@atsro.co.kr).

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## I. INTRODUCTION

RECONFIGURABLE intelligent surfaces (RISs) have emerged as a promising technology due to their large-scale wave manipulation capabilities and cost efficiency [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. An RIS typically consists of 2-D periodically patterned metal structures on a grounded substrate, integrated with tunable components such as liquid crystals (LCs), p-i-n diodes, and varactor diodes for implementing phase shifters [11], [12], [13], [14], [15], [16], [17].

Each tunable component offers distinct advantages and disadvantages. For example, p-i-n diodes are inexpensive, current-driven, and operate at low voltages. However, they tend to generate significant heat due to the high current requirement. Therefore, the p-i-n diode consumes more power than other components at the unit cell level. For instance, the MADP-000907-14020 model, which is commonly used in the literature, requires 10 mA and 2.5 V to drive a single cell—significantly higher power consumption compared to LC or varactor diodes [7]. In contrast, varactor diodes are voltage-driven and produce less heat, but they are generally more expensive and have limited operational frequency ranges. LCs support continuous phase tuning over a wide frequency spectrum—from direct current (dc) to optical frequencies—and, being voltage-driven, also exhibit low heat dissipation. Due to these favorable characteristics, this work adopts an LC-based phase shifter for RIS wave manipulation. In general, the response remains stable at temperatures below 100 °C; therefore, stability with respect to temperature is ensured [18].

From a power consumption perspective, different tunable components exhibit varying demands. p-i-n diodes operate at low voltages but require high current, necessitating driver circuits capable of delivering sufficient current. Conversely, components such as varactors or LCs typically require higher bias voltages (often exceeding 20 V) but draw minimal current. When total power consumption—including that of the driver circuit—is considered, p-i-n diodes may actually offer greater efficiency compared to varactor diodes [18]. While previous studies have investigated RIS power consumption [19], [20], their focus has primarily been on modeling. For instance,

Tesmer et al. [18] proposed a power model for RISs utilizing p-i-n or varactor diodes. However, strategies to actively reduce power consumption have not yet been thoroughly explored.

This study addresses the challenge of minimizing RIS power consumption. The total power consumption of an RIS can be divided into two components: power drawn by the control circuit ( $P_c$ ) and power dissipated by the unit cells ( $P_u$ ). To reduce the overall power consumption, this article proposes a novel architecture that significantly lowers control circuit power by employing switches and capacitors activated through bias pulses.

Furthermore, the use of LCs as the tunable element reduces the power dissipation in the unit cells to a negligible level.

A key feature of the proposed method is its ability to maintain beam sustainability. This is enabled by a customized circuit design in which capacitors store charge, allowing the established beamforming state to persist even after the power supply is turned off. This innovative approach represents a significant advancement toward the development of energy-efficient RISs. In addition to power modeling, this study introduces a significantly simplified bias network. Most RIS configurations require complex biasing networks to enable 2-D beamforming. In a reflective array (RA) composed of  $N \times N$  cells, conventional designs require  $N \times N$  biasing nodes [21], [22], [23], [24]. As the electrical size of the RIS increases to relay more power to users, the biasing circuitry becomes more intricate. Traditional biasing topologies can be classified into passive or direct addressing schemes, where each cell corresponds to one bias node, leading to  $N \times N$  control points. In contrast, this work employs an active addressing scheme, which reduces the number of required bias nodes to just  $2N$  for an  $N \times N$  array by incorporating switches and capacitors. To the best of the authors' knowledge, no prior studies have implemented such an active addressing scheme in RIS architectures.

To realize electrically large RIS arrays that can efficiently relay substantial power to users, scalability must be achieved alongside low-power consumption. The proposed RIS module addresses this by significantly reducing the power required for both beamforming and beam-holding. Capacitors embedded in the bias circuit retain the established beam state without continuous power consumption, enabling quasi-permanent beamforming. This contributes to ultralow-power operation. In this study, the LC was selected as the tunable element due to its continuous phase response, voltage-driven operation, and inherently low-power consumption. Since the LC is controlled by voltage pulses rather than continuous current, the charge stored in the capacitors is retained for extended periods due to a high time constant. The performance of the proposed RIS module was evaluated in three aspects: antenna performance, power consumption, and link testing. In the antenna characterization, the 3 dB beam coverage was measured to be  $0^\circ$  to  $+40^\circ$  in the blocked plane and  $\pm 40^\circ$  in the unblocked plane for both polarizations. The aperture efficiency and sidelobe level (SLL) were 23.7% and  $-13$  dB, respectively. In the power consumption test, the beamforming operation consumed approximately 2.1 W. Remarkably, in the beam-holding test,

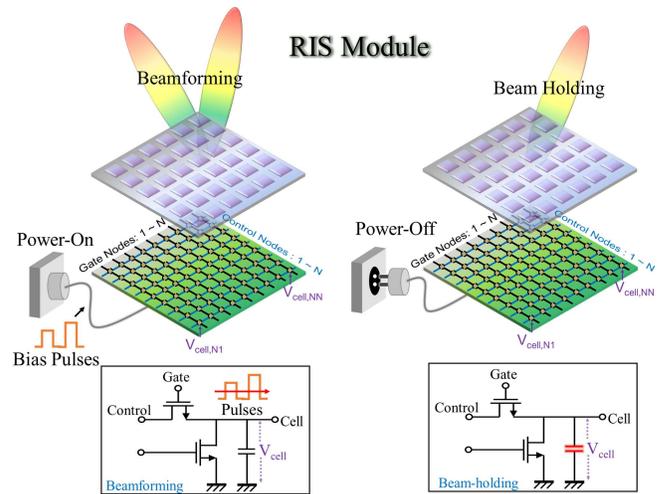


Fig. 1. Two modes of the proposed RIS.

the beam state was maintained for more than four days without any dc power supply. Finally, a link test was conducted using millimeter-wave (mmWave) 5G-standard modulation signals to validate the feasibility of the proposed RIS module for fixed wireless communication applications.

This article is organized as follows: Section II-A introduces and discusses the design structure and operating principle of the proposed RIS unit cell. Section II-B details the bias configuration of the RIS module. Section III-A presents the integration of the LC-based RIS unit cell with the biasing circuit. Section III-B discusses power modeling, the measurement setup, and the experimental results of 2-D beam scanning and beam holding. Finally, conclusions are drawn in Section IV.

Compared to the conference version of this work [25], several important extensions have been made. First, the principles and structural details of the LC unit cells are described in greater depth. In addition, the overall RIS module architecture is explained more comprehensively. A new comparative table has also been included to benchmark our design against previous RIS studies, highlighting distinctive aspects such as beam-holding functionality and estimated peak power consumption. Finally, a more detailed discussion on power consumption and beam holding is provided, where equivalent circuit models and time-constant analysis are introduced. It is also demonstrated that variations in LC capacitance under dc bias have negligible influence on the system performance.

## II. PROPOSED RIS MODULE

### A. LC-Based RIS Unit Cell and Bias Circuit Cell

Fig. 1 illustrates the two operational modes of the proposed LC-based RIS: the beamforming mode, in which bias pulses are applied to configure the beam, and the beam-holding mode, in which the configured beam is maintained even after the bias power is turned off. Laboratory-level beam-holding and power consumption tests confirmed that the beam could be sustained for up to four days without any dc power supply, and power is only consumed during the initial beamforming phase. This characteristic enables a drastic reduction in power consumption compared to conventional relay-based solutions.

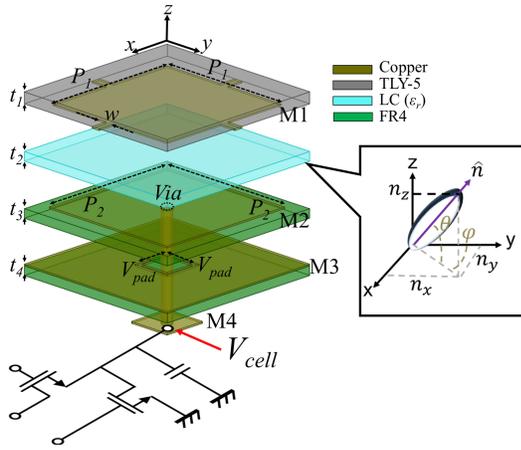


Fig. 2. Exploded view of the proposed unit cell.

Fig. 2 depicts an exploded view of the unit cell of the proposed RIS unit cell. Taconic TLY-5 and FR4 are used as the substrates for the unit cells. An M1 metallic patch is placed beneath the TLY-5 layer to resonate within the targeted frequency band of 27–30 GHz for radio frequency (RF) operation, and it is also connected to serve as a dc bias ground. The M2 metallic layer, which is connected to the bias circuit via a metal via, delivers the bias signal to the LC material. An open M3 metal ground effectively isolates the RF signals between the bias circuit and the unit cell. The bottom of the unit cell is connected directly to the bias circuit. The detailed operating principle of the circuit will be described later. The periodicity of the unit cell is 4 mm. The dielectric constant and loss tangent of the TLY-5 substrate are 2.2 and 0.0009, respectively, and those of the FR4 substrate are 4.4 and 0.02. The relative permittivity of the LC material is complex ( $\epsilon'_{LC} - j\epsilon''_{LC}$ ) due to its intrinsic losses. According to the datasheet, the tunable dielectric constant of the LC material used in this study ranges from 2.5 to 3.5 (corresponding to  $\epsilon_{\perp}$  to  $\epsilon_{\parallel}$ ). The thicknesses of the layered substrates  $t_1$  through  $t_4$  are 0.25, 0.2, 0.2, and 0.2 mm, respectively. The molecules of the LC used in this study are represented by the structure shown in Fig. 2, and their orientation is described by the components  $n_x$ ,  $n_y$ , and  $n_z$ . When quasistatic electric fields are applied within the LC, the interaction between the field and the molecules causes the directors to reorient, and the resulting second-order tensor permittivity is given as follows:

$$\bar{\bar{\epsilon}}_r(\bar{r}) = \epsilon_{\perp} \bar{\bar{I}} + \Delta\epsilon_r \bar{\bar{N}}(\bar{r}). \quad (1)$$

Here,  $\bar{\bar{I}}$  denotes the second-order identity tensor,  $\Delta\epsilon_r = \frac{\epsilon_{\parallel}}{\epsilon_{\perp}} - \epsilon_{\perp}$  represents the dielectric anisotropy of the LC, and  $\bar{\bar{N}} = \hat{n}(\bar{r}) \otimes \hat{n}(\bar{r})$  is the second-order dyadic tensor formed by the outer product of the unit vector  $\hat{n}(\bar{r})$  with itself. The unit vector  $\hat{n}(\bar{r})$  is defined macroscopically as the average orientation of LC molecules within the local region.

When an external quasistatic electric field  $E_b$  is applied from the outer circuit to the LC cavity, the electrostatic energy is converted into elastic energy within the LC medium, causing the molecules to reorient. This process is governed by the minimization of the total free energy, comprising both Frank–Oseen elastic and electrostatic components, which lead

to a reorientation of the LC director vector  $\hat{n}$ . The external field  $E_b$  is applied by outer circuit. Accordingly, based on the applied bias voltage, the relationship described in (1) can be explicitly represented as in the following equation:

$$\bar{\bar{\epsilon}}_r = \begin{pmatrix} \epsilon_{\perp} & 0 & 0 \\ 0 & \epsilon_{\perp} & 0 \\ 0 & 0 & \epsilon_{\perp} \end{pmatrix} + \Delta\epsilon_r \begin{pmatrix} n_x n_x & n_x n_y & n_x n_z \\ n_y n_x & n_y n_y & n_y n_z \\ n_z n_x & n_z n_y & n_z n_z \end{pmatrix}. \quad (2)$$

Assuming symmetry structure and equivalent effective permittivity, the effective permittivity tensor can be simplified by diagonal form as expressed in the following equation:

$$\epsilon_{\text{eff}} = \text{diag}(\epsilon_{xx}, \epsilon_{yy}, \epsilon_{zz}). \quad (3)$$

According to the molecular rotation, the three components can be expressed in terms of the rotation angle  $\theta$  and  $\varphi$  as follows:

$$\epsilon_{xx} = \epsilon_{\perp} + \Delta\epsilon_r \sin^2 \theta \cos^2 \varphi \quad (4)$$

$$\epsilon_{yy} = \epsilon_{\perp} + \Delta\epsilon_r \sin^2 \theta \sin^2 \varphi \quad (5)$$

$$\epsilon_{zz} = \epsilon_{\perp} + \Delta\epsilon_r \cos^2 \theta. \quad (6)$$

Therefore, the reflection coefficient of the LC-based unit cell can be expressed in the following equation:

$$S_{11}(\bar{\bar{\epsilon}}_r) = \frac{Z_{uc}(\bar{\bar{\epsilon}}_r) - Z_0}{Z_{uc}(\bar{\bar{\epsilon}}_r) + Z_0}. \quad (7)$$

In this context,  $Z_{uc}$  and  $Z_0$  represent the impedances of the unit cell and free space, respectively. Notably,  $Z_{uc}$  depends on the anisotropic permittivity tensor of the LC. In the full-wave simulator,  $Z_{uc}$  is evaluated by incorporating the anisotropic permittivity described by (4)–(6); therefore, the reflection phase can be controlled through variations in the permittivity.

Fig. 3 shows the frequency responses of the magnitude for various dimensions of  $P_1$  and  $P_2$  in the M1 and M2 layers. Two resonance points are observed, corresponding to M1 and M2 layers, respectively.  $P_1$  primarily affects the upper band due to the presence of adjacent low-permittivity substrates, including LC and TLY-5. In contrast,  $P_2$  influences the lower band and exhibits higher loss as a result of the adjacent lossy and high permittivity material, FR4. As the dimension increases, the corresponding resonance point in each case shifts toward lower frequencies. The final dimensions of the M1 metallic patch are  $3.2 \times 3.2$  mm, while those of the M2 layer are  $3.7 \times 3.7$  mm.

Fig. 4 illustrates the simulated magnitude and phase responses as functions of frequency for two extreme LC states ( $\epsilon_{\perp}$  and  $\epsilon_{\parallel}$ ).

The simulations were carried out using the Floquet mode setup in Ansys HFSS. At 28 GHz, the maximum reflection loss was 3.5 dB, and the maximum phase shift achieved was  $279^\circ$ . In Fig. 4, black and red curves indicate the magnitude and phase responses, respectively, while solid and dashed lines represent the  $\epsilon_{\perp}$  and  $\epsilon_{\parallel}$  states, respectively. Due to the wide-area coverage requirement of RISs, maintaining response stability across varying angles of incidence is essential.

Fig. 5 shows the simulated magnitude responses as functions of frequency for various angles of incidence and different values of the dimension parameter  $P_2$ . Consideration of angle of incidence in unit cell simulations is essential, as it reveals

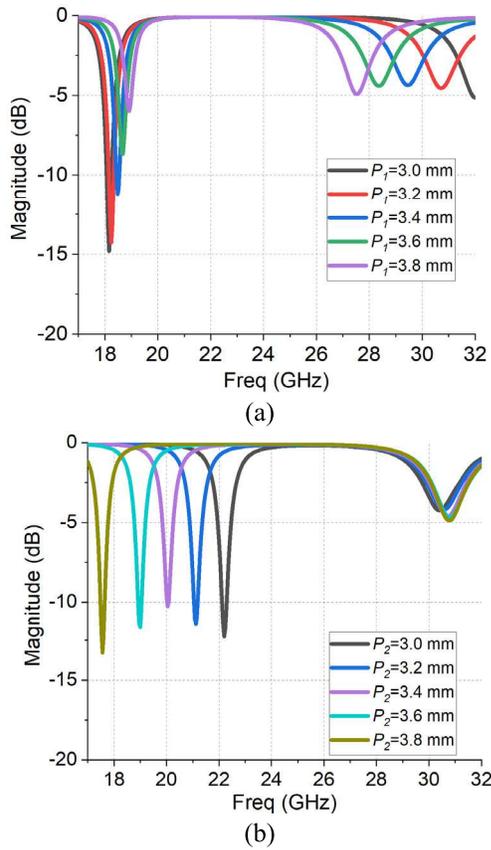


Fig. 3. Frequency responses of magnitude for various dimensions of (a)  $P_1$  and (b)  $P_2$ .

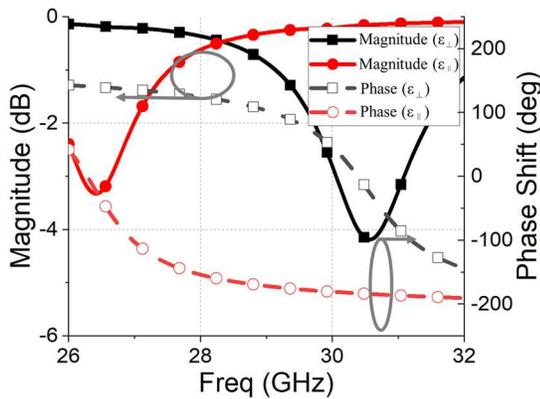


Fig. 4. Magnitude and phase of frequency responses for two extreme LC states.

the angular stability of the structure and indicates how performance changes under oblique illumination, which is critical for practical beam steering and wide-angle operation. Although  $P_2$  was originally introduced to facilitate the excitation of the LC layer, it was observed that smaller values of  $P_2$  result in undesired resonances as the angle of incidence increases. Therefore,  $P_2$  must be sufficiently large to suppress these resonance effects and ensure stable operation under oblique incidence.

Fig. 6 illustrates the schematic of the proposed bias circuit, its operational sequence, and the corresponding simulation results for two representative unit cells. As shown in Fig. 2,

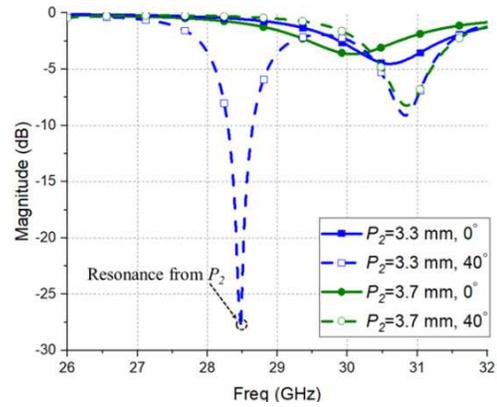


Fig. 5. Frequency responses of magnitude responses as a function of angle of incidence for various dimensions of  $P_2$ .

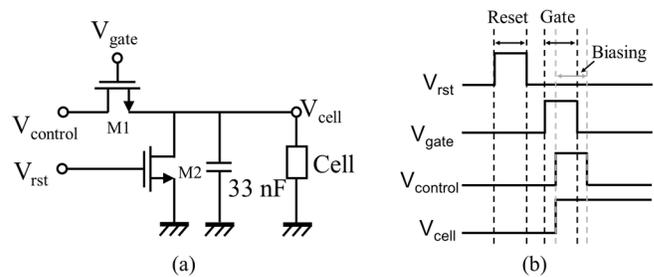


Fig. 6. (a) Schematic of the bias circuit and (b) operation diagram.

the bias circuit is integrated at the bottom node of the unit cell. The circuit consists of two MOS transistors (M1 and M2) and a single capacitor. The M1 transistor connects  $V_{control}$  to  $V_{cell}$  and operates as a switch controlled by  $V_{gate}$ . Fig. 6(b) depicts the operational timing diagram. When  $V_{gate}$  is in the high state, current flows from  $V_{control}$ , charging the capacitor and establishing a voltage at the  $V_{cell}$  node. Since the LC-based RIS connected to  $V_{cell}$  behaves as an open patch structure (effectively a shunt capacitor), the established voltage is retained even after M1 and M2 are turned off. To reconfigure the bias state of the LC-based RIS unit cell, a different voltage must be applied at  $V_{cell}$ . However, if a residual voltage remains from a previous state, a reverse current may be induced depending on the potential difference between  $V_{cell}$  and  $V_{control}$ . To mitigate this, an initialization step is required to reset  $V_{cell}$  to zero prior to applying a new control voltage. For this purpose, the M2 transistor is connected in parallel with the storage capacitor. By applying a reset signal  $V_{rst}$ , M2 discharges the capacitor, thereby resetting  $V_{cell}$  to zero and enabling reliable initialization with a simple circuit configuration.

Fig. 7 presents the simulation results for two arbitrary unit cells controlled by the proposed bias circuit. Upon applying control voltages in the range of 5–20 V, each cell successfully established its bias voltage. Once a bias pulse is applied, the capacitor sustains the voltage, enabling beam-holding. Furthermore, it was confirmed that applying the reset signal correctly discharged all cells, resetting their voltages to zero as intended. The settling time is within approximately 3 ns, which is significantly faster than the molecular reorientation

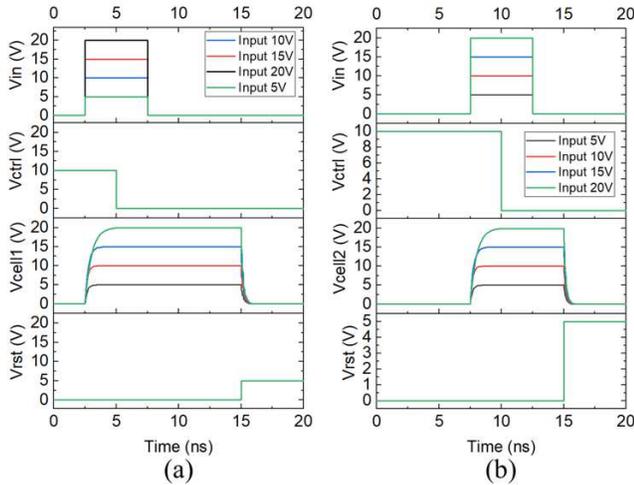


Fig. 7. Circuit simulation results. [(a) cell-1 and (b) cell-2].

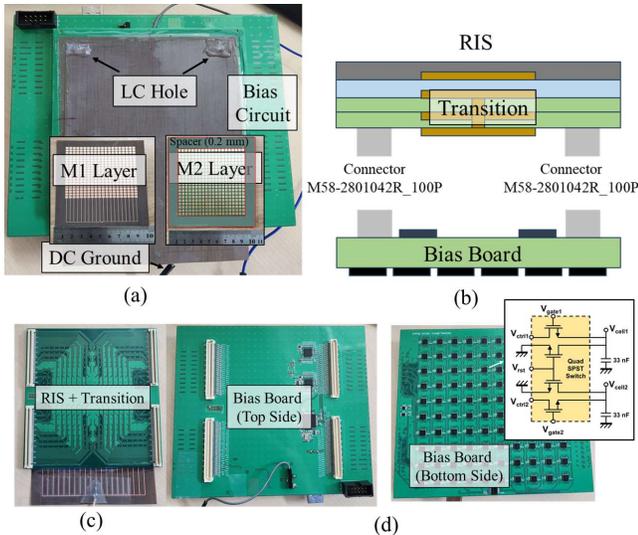


Fig. 8. Structure and implementation of the proposed LC-based RIS module: (a) photograph of the fabricated RIS module; (b) cross-sectional schematic of the module; (c) rear view of the RIS-transition assembly; and (d) front and back side views of the bias board.

time of the LC. Therefore, it does not impose any limitation on the beamforming speed. The proposed addressing method may impose latency as the array size increases. Although this latency scales approximately linearly with the number of addressed elements, the absolute delay for a full-array update remains minimal. Furthermore, parallel addressing schemes, such as row-column multiplexing, could be employed in future designs to further mitigate latency in larger arrays.

### B. Realization of the Proposed RIS Module

This section describes the realization of the proposed LC-based RIS module, which integrates the unit cell array with the bias circuit. Fig. 8(a) shows the detailed view of the fabricated prototype. The RIS module was implemented as a  $20 \times 20$  array to validate the proposed addressing scheme for a large-scale RIS configuration. LC holes were introduced to allow injection of the LC material into the cavity. The cavity was formed by sandwiching a 0.13 mm thick TLY-

5 spacer and securing it with double-sided adhesive tape. When two layers of tape were used, the total cavity thickness increased by 0.7 mm. To prevent LC leakage, the injection holes were sealed using epoxy. The top layer of the RIS module was covered with TLY-5, while the M1 layer and dc ground pad were located on the backside of the substrate. The active radiating area of the RIS measured  $80 \times 80$  mm, while the overall dimensions, including the bias circuit, were  $135 \times 150$  mm. The FR4 layers, which included the M2 layer and the transition board for bias signal delivery, were fabricated using standard PCB processes. Fig. 8(b) presents a simplified cross-sectional view of the assembled sample of the RIS and transition board. M58-2801042R\_100P connectors are employed to integrate the assembled sample and the bias board. This structure enables a compact and scalable configuration suitable for millimeter-wave operation. Fig. 8(c) shows the bottom and top views of the assembled sample and the bias board. The top layer of the bias board includes connectors and digital control components (e.g., microcontrollers or shift registers) and contains analog switch arrays and storage capacitors. The integrated RIS-transition structure is designed to interface with the bias board through connectors, enabling straightforward electrical control of the unit cells. Each LC cell receives a short bias pulse through these switches, after which the charge is retained by the capacitor, allowing beam-holding operation without continuous power supply. Fig. 8(d) presents the backside view of the bias board. The Vishay DG441B analog switch (QFN-16 package), fabricated using a high-voltage CMOS process, was selected as the control chip due to its compatibility with the typical LC bias voltage range of 0–20 V. The die area of such analog switches is typically on the order of  $\sim 1$  mm<sup>2</sup>, as inferred from comparable ICs of the same generation. The chip's breakdown voltage (44 V) exceeds this range, providing sufficient operational margin and reliability. After completing the postfabrication processes—including LC injection, epoxy sealing, and soldering—the LC-based RIS module and bias board were integrated using board-to-board connectors.

## III. DISCUSSION ON MEASUREMENT RESULTS

### A. Antenna Performance

Although the proposed LC-based RIS is intended for reconfigurable electromagnetic wave manipulation, it is crucial to verify its antenna characteristics to confirm that the structure can operate reliably in radiative environments; therefore, this section details the measurement setup and results pertaining to its antenna performance.

Fig. 9 illustrates the measurement setup used to evaluate the performance of the proposed LC-based RIS module. All measurements were conducted in an anechoic chamber. The  $S$ -parameters used to derive the phase-voltage characteristics were measured using a vector network analyzer (VNA), while the beam pattern measurements were performed using a vector signal generator and a spectrum analyzer. The feed antenna was positioned according to the criterion of maximum feed efficiency, as described in [11]. The feed configuration strongly influences RIS performance. An on-axis feed provides symmetric illumination with low SLL, but suffers from blockage

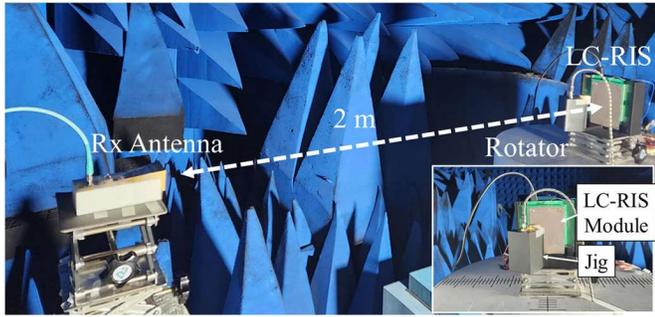


Fig. 9. Measurement setup for antenna performance of the proposed structure.

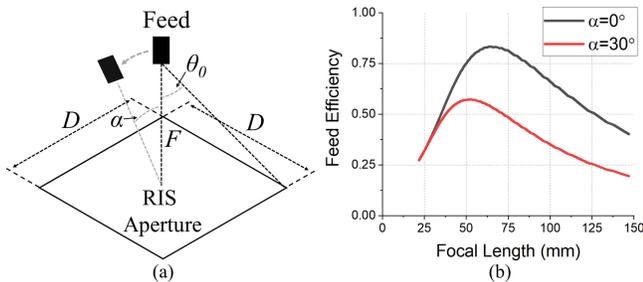


Fig. 10. (a) Configuration of feed antenna and (b) calculated feed efficiencies for different offset angles.

and multiple reflections. An offset feed avoids blockage, yet introduces asymmetric illumination that increases spillover, raises SLL, and broadens or tilts the main beam. The 3-dB beamwidth is inversely proportional to the effective aperture size: larger  $F/D$  ratios weaken edge illumination and broaden the beam, while smaller  $F/D$  ratios strengthen edge illumination, narrowing the beam but potentially increasing SLL. In practice, quantization effects further degrade performance. Limited phase resolution across the aperture reduces efficiency, broadens the beam, lowers gain, and elevates SLL. These effects are amplified in offset-feed configurations, where asymmetric illumination already degrades aperture efficiency. Therefore, both feed placement and phase quantization must be jointly optimized to achieve high efficiency and controlled radiation characteristics. The optimum focal length is determined at the point where the feed efficiency, defined as the product of taper and spillover efficiencies, excluding radiation efficiency, reaches its maximum. Taper efficiency accounts for the degradation caused by nonuniform illumination across the aperture, while spillover efficiency denotes the fraction of feed power captured by the aperture. Fig. 10(a) illustrates the feed layout and RIS aperture used to calculate the feed efficiency for the optimal focal length. The definitions in the figure follow those in [26]. The taper and spillover efficiencies can be evaluated as follows. First, the symmetric feed power pattern is modeled as in (8)

$$G_{\text{feed}} = \cos^n \theta. \quad (8)$$

As the antenna 3-dB beamwidth decreases, the parameter  $n$  increases. Moreover, when the feed antenna is placed at an offset angle  $\alpha$ , the illumination becomes asymmetric, requiring an optimized feed pattern [27]. Under this condition, the

feed pattern  $\cos \psi(\theta, \phi)$  can be reformulated as given in the following equation:

$$\cos \psi(\theta, \phi) = \cos \theta \cos \alpha + \sin \theta \sin \alpha \sin \phi. \quad (9)$$

By employing this equation, the taper and spillover efficiency are calculated as correspondingly expressed in the following equations:

$$\eta_{\text{spill}} = \frac{\int_0^{2\pi} \int_0^{\theta_0} \cos^n \psi(\theta, \phi) \sin \theta d\theta d\phi}{\frac{2\pi}{n+1}} \quad (10)$$

$$\eta_{\text{taper}} = \frac{\left| \int_0^{2\pi} \int_0^{\theta_0} \cos^{n/2} \psi(\theta, \phi) \sin \theta d\theta d\phi \right|^2}{2\pi (1 - \cos \theta_0) \int_0^{2\pi} \int_0^{\theta_0} \cos^n \psi(\theta, \phi) \sin \theta d\theta d\phi} \quad (11)$$

where  $\theta_0$  is defined as the half-subtended angle between the antenna axis and the line from the feed to the aperture edge, given by the following equation:

$$\tan \theta_0 = \left( \frac{D}{2} \right) / F. \quad (12)$$

Here,  $D$  denotes the side length of the square aperture and  $F$  is the focal length. However, in some formulations,  $D$  is alternatively defined as the diagonal length of the aperture. In this study, a horn antenna with a gain of 13.5 dBi is employed, corresponding to an exponent  $n$  of 13.

Fig. 10(b) presents the calculated feed efficiency for different offset angles. As shown in Fig. 10(b), when the offset angle  $\alpha$  is  $0^\circ$ , the feed efficiency is high, and the optimum focal length is calculated at a relatively larger distance from the aperture. However, at  $\alpha = 30^\circ$ , the feed efficiency decreases, and the optimum focal length shifts closer to the aperture due to the unbalanced illumination and increases spillover caused by the offset configuration. In this study, an offset angle of  $30^\circ$  and a focal length of 50 mm are selected as the feed configuration in order to reduce blockage of the broadside beam.

To achieve beamforming, the phase-voltage response of the LC material must be characterized. Fig. 11(a) presents both simulated and measured phase responses for varying permittivity and voltage values. In the simulation, the frequency range was set from 24 to 32 GHz to observe the phase shift corresponding to changes in the LC relative permittivity ( $\epsilon_r$ ) from 2.5 to 3.5. Within the target frequency band of 27–30 GHz, a phase shift exceeding  $200^\circ$  was achieved. In the measurement, phase differences corresponding to applied voltages in the range of 0–10 V were extracted based on (13), validating the LC's tunability for practical beamforming applications

$$\varphi_{\text{difference}} = \varphi_V - \varphi_0. \quad (13)$$

Here,  $\varphi_0$  denotes the phase when none of the unit cells are biased, while  $\varphi_V$  represents the phase when all unit cells are biased at a specific voltage level. Fig. 11(b) presents bar charts comparing the simulated and measured phase responses within the frequency range of 27–30 GHz. The measured phase range is slightly smaller than the simulated one, which can be attributed to variations in spacer thickness, the presence of air bubbles within the LC cavity, and partial epoxy permeation affecting the dielectric environment.

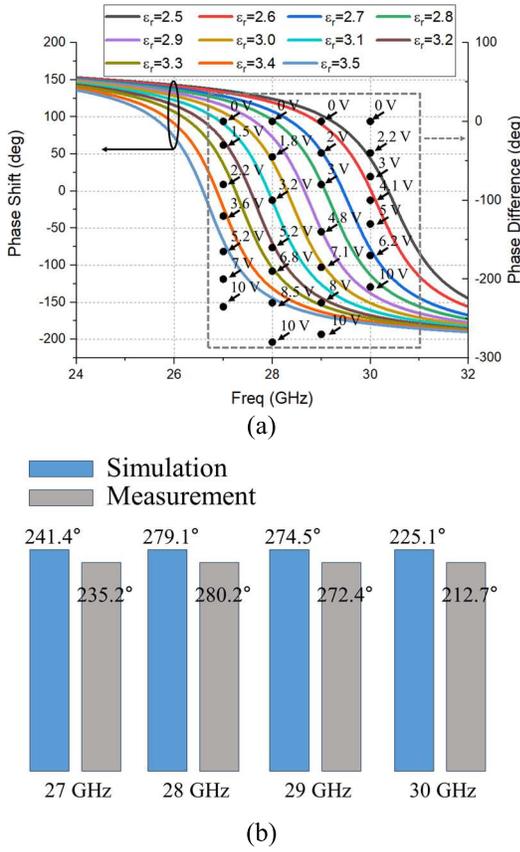


Fig. 11. Simulated (solid) and measured (dots) reflection-phase responses. (a) Phase vs. frequency for  $\square$  with  $V_{\text{bias}}$ -labeled measurements; dashed box: operating band. (b) Phase-tuning range (max–min) in the band for simulation and measurement.

Fig. 12 shows the simulated and measured far-field beam patterns obtained using the extracted phase–voltage relationship. Beamforming was achieved by applying six distinct voltage states to the LC-based RIS, corresponding to different phase profiles across the surface. Both  $E$ - and  $H$ -plane beam patterns were measured to validate the 2-D beam-scanning capability of the proposed LC-based RIS module. In the  $H$ -plane, the beam patterns were measured over a limited angular range of  $0^\circ$ – $40^\circ$  due to physical blockage caused by the feed antenna and mounting jig. In contrast, the  $E$ -plane measurements confirmed full angular coverage from  $-45^\circ$  to  $+40^\circ$ . In the  $E$ -plane, the measured gain ranged from 19.8 to 22.2 dBi, with the lowest observed SLL at  $-13$  dB. For the  $H$ -plane, the measured gain ranged from 16.2 to 21.23 dBi, with the lowest SLL recorded at  $-11$  dB.

The reduction in gain in the  $H$ -plane is attributed to partial obstruction introduced by the jig during measurement. The maximum aperture efficiency was determined to be 23.7% at 28 GHz in the  $E$ -plane. In addition, a 6 dB gain bandwidth spanning 27–30 GHz was confirmed within the beam coverage range, demonstrating the wideband beamforming capability of the proposed RIS. The aperture efficiency was obtained by calculating following equation:

$$\eta_{\text{ap}} = \frac{G}{4\pi A/\lambda_0^2}. \quad (14)$$

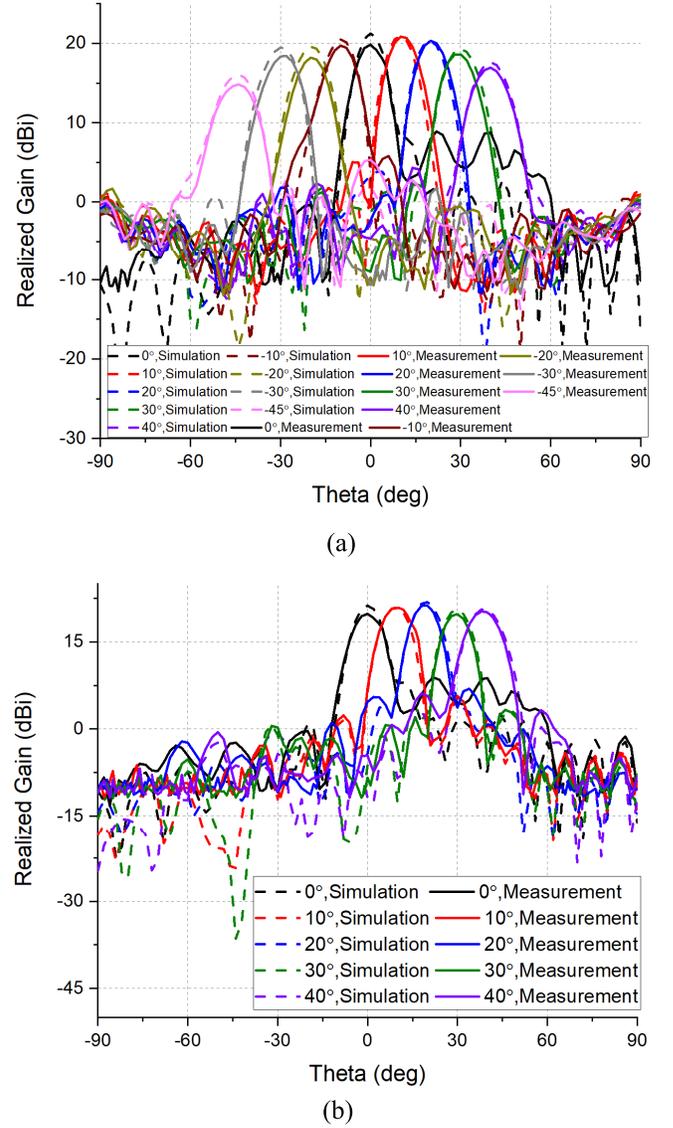


Fig. 12. Measured and simulated beam patterns @ 28 GHz in (a)  $E$ -plane and (b)  $H$ -plane (solid: measurement, dashed: simulation).

Here,  $\lambda_0$  represents the free-space wavelength at 28 GHz, and  $A$  denotes the aperture area of the RIS. Based on the measured maximum gain of 22.2 dBi, the maximum aperture efficiency is calculated to be 23.7%. The beam coverage ranges from  $0^\circ$  to  $62^\circ$ . The waves reflected toward the feed antenna were degraded because of the blockage.

It should be noted that in our measurement setup, the feed radiation pattern extended into negative  $H$ -plane angles, which limited the full demonstration of 2-D beamforming. This effect is attributed to the measurement configuration rather than the RIS structure itself and can be mitigated by optimizing the feed arrangement or modifying the measurement setup. Such improvements will be considered in future work to fully validate the 2-D beamforming capability. Both simulation and measurement results show a degree of beam asymmetry. This effect is primarily attributed to the offset-feed configuration, which inherently introduces uneven illumination across the aperture and thus appears in both simulation and measurement. In the measurement, the asymmetry is further accentuated by

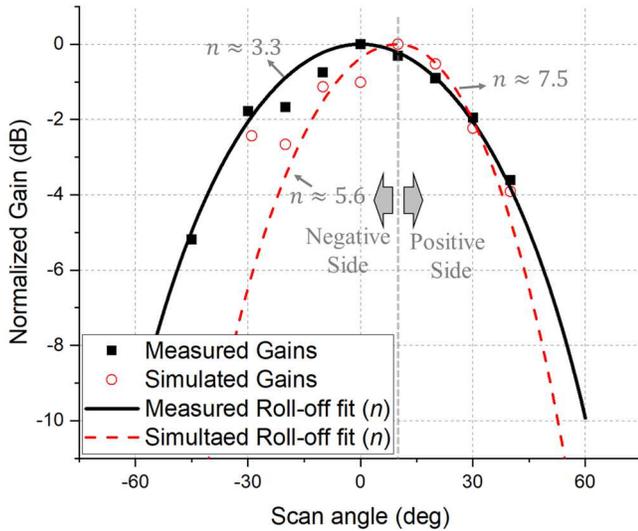


Fig. 13. Roll-off patterns of the measured and simulated results at 28 GHz, normalized to the maximum gain.

feed blockage, mounting structures, and fabrication tolerances of the LC cavity.

Fig. 13 illustrates the roll-off patterns of the measured and simulated results at 28 GHz, with each curve normalized to the maximum gain. In the measured case, the peak gain occurred at  $10^\circ$ , producing an offset in the roll-off configuration. On the positive scan side, the measured roll-off follows a  $\cos^n\theta$  dependence with  $n \approx 7.5$ . In contrast, the negative side exhibits a noticeable mismatch with the simple  $\cos^n\theta$  approximation, mainly due to the offset-feed illumination and partial blockage in the measurement setup. The simulated roll-off, however, is well described by a symmetric  $\cos^n\theta$  curve with  $n \approx 3.3$ .

### B. Beam-Holding

This section presents the beam-holding performance of the proposed LC-based RIS module. Beam-holding refers to the ability of the RIS to maintain a formed beam after the application of bias pulses, even when the power supply is turned off or no further control actions are applied. This feature is particularly important for ultralow-power applications, as it allows the beam to persist without continuous power consumption. In contrast, active beamforming requires instantaneous power input to reconfigure the phase profile when needed.

The beam-holding capability is especially well-suited for fixed wireless access (FWA) scenarios, where expanding communication coverage is desired without deploying additional base stations or repeaters. To evaluate this capability, the beam-holding test was conducted immediately after beamforming was successfully established. No further electrical control was applied, and the formed beam was maintained continuously for four days without any power supplied to the bias circuit.

Fig. 14 compares the instantaneous and beam-holding radiation patterns, which exhibit a high degree of similarity. The slight discrepancies observed between the two patterns may be attributed to cable movement, equipment heating, or internal displacement of the LC within the cavity. To evaluate the

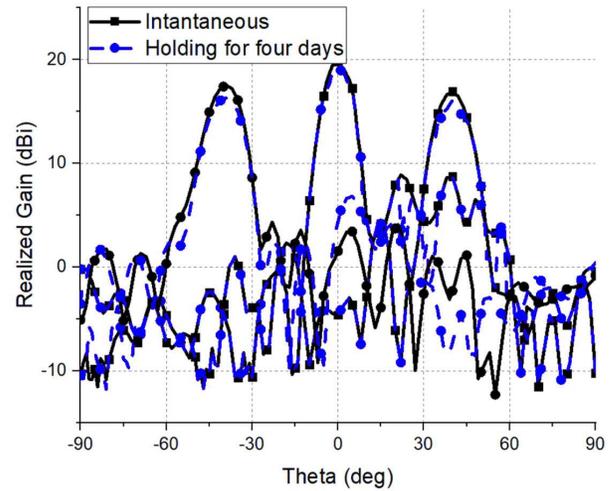


Fig. 14. Measurement results for beam-sustainability (solid: instantaneous and dashed: four days long).

beam-sustainability of the proposed RIS, a continuous beam-holding experiment was conducted for four days without any dc power supply.

This duration was chosen as a practically manageable period to verify the long-term stability of the capacitor-based biasing scheme under laboratory conditions. The formed beam was successfully maintained throughout the test, and subsequent re-biasing and re-measurement confirmed that the RIS performance remained consistent with the initial state, indicating that prolonged dc biasing did not cause any permanent damage or degradation of the LC or the unit cells. The time constant  $\tau$  of the charging/discharging circuit is defined by the effective resistance  $R_{\text{eff}}$  and effective capacitance  $C_{\text{eff}}$  as  $\tau = R_{\text{eff}}C_{\text{eff}}$ . When a gate and effective capacitance  $C_{\text{eff}}$ , as given by  $\tau = R_{\text{eff}}C_{\text{eff}}$  and when the gate voltage is in the high state,  $R_{\text{eff}}$  approaches zero due to the formation of a low-resistance channel in the MOS transistor, enabling rapid charging of the capacitor. Conversely, when the gate is in the low state,  $R_{\text{eff}}$  becomes significantly large, effectively preventing discharge and thereby sustaining the voltage across the LC. As a result, the charging time is governed primarily by the intrinsic response time of the LC under high gate voltage, while the discharging time is determined by the electrical properties of the holding circuit under low gate voltage. Furthermore, as the LC is driven by a dc bias, its response speed remains constant within the operating frequency band.

Table I compares key performance metrics of LC-based RISs from prior works and the proposed design. Operating at 28 GHz, the proposed RIS achieves the highest aperture efficiency (23.7%) among the listed studies. It supports 2-D scanning with an  $85^\circ$  coverage and a phase shift range of  $275^\circ$ , comparable to state-of-the-art designs. Unlike previous works, it features beam-holding capability, maintaining the beam without continuous power. The required bias level is just 10 V, which is significantly lower than in [19] and [23]. Thanks to the active addressing scheme, only 40 bias nodes are needed for the  $20 \times 20$  array, the lowest among all. These results demonstrate that the proposed RIS achieves high efficiency,

TABLE I  
PERFORMANCE COMPARISON OF RIS IN VARIOUS STUDIES

Feature	[19]	[21]	[19]	[23]	This work
Frequency [GHz]	3.5	23.8	3.5	37.5	28
Aperture Efficiency [%]	N.A.	2.6	N.A.	-	23.7
SLL [dB]	N.A.	-	N.A.	-14	-13
Scanning Capability	1D	1D	1D	2D	2D
Coverage (°)	N.A.	60	N.A.	40	85
Array	20 × 20	26 × 38	20 × 20	12 × 12	20 × 20
Max. Phase Shift Range [°]	N.A.	150	N.A.	338	275
Maximum Bias Level [V]	2	11	20	36	10
Beam-Holding Capability	N.A.	N.A.	N.A.	N.A.	YES
# of Bias Nodes	400	26	400	144	40
Tunable Component	PIN	LC	Varactor	LC	LC
*Estimated Maximum Power Consumption [W]	10	N.A.	180	N.A.	2.15

\*Power consumption was calculated on a 20 × 20 array configuration

TABLE II  
BREAKDOWN OF THE APERTURE EFFICIENCY COMPONENTS OF THE PROPOSED RIS

Stages	Features	Efficiencies [%]
Unit cell	Reflection Magnitude	85.2
	Reflection Phase	92.1
Feed Configuration	Taper	63.7
	Spillover	89.1
	Edge	93.5
RIS Module	Polarization	99.2
	Blockage	79.3
	Etc.	68.0
Total	-	23.7

reduced complexity, and low-power consumption, making it highly suitable for practical fixed wireless applications.

Table II presents the breakdown of the aperture efficiency of the proposed RIS, grouped into three categories: unit-cell, feed-configuration, and RIS-module efficiencies. At the unit-cell level, the reflection efficiency corresponds to the average reflected power from the elements, while the phase efficiency accounts for the limited phase dynamic range and quantization effects.

For the feed configuration, the taper efficiency describes the uniformity of the illumination amplitude across the aperture, the spillover efficiency represents the fraction of feed power intercepted by the aperture, and the edge efficiency decreases as diffracted fields at the aperture boundary increase. At the RIS-module level, the polarization efficiency is defined as the ratio of co-polarized to total co- and cross-polarized power, the blockage efficiency accounts for scattering blocked by the feed antenna, and additional terms such as fabrication imperfections and mutual coupling are included as other losses. The overall aperture efficiency is then obtained as the product of all these factors. The definitions employed in this work follow the methodology reported in [28].

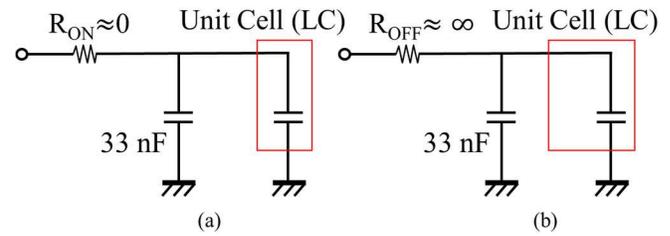


Fig. 15. DC equivalent circuit of the unit cell in the RIS module. [(a) switch on and (b) switch off].

Fig. 15 illustrates the equivalent circuit of the system, including the RIS unit cell, under switch on and off conditions. To explain the beam-holding principle using the equivalent circuit, the RIS unit cell is modeled as a shunt combination of a resistor and a capacitor. When a voltage pulse is applied to the gate, the switch turns on and is modeled as a low resistance. This results in a low time constant, enabling fast charging of the capacitor. Conversely, when the gate pulse is turned off, the switch is modeled as a very high resistance, leading to a high time constant and effectively preventing discharge. This mechanism explains how beam-holding is achieved using the proposed pulse-based approach, as the capacitor retains the bias voltage across the RIS unit cell for an extended period without continuous power supply. The effective capacitance of the patch antenna can be approximated using the parallel-plate capacitor model

$$C_{LC} = \epsilon_r \epsilon_0 \frac{A_{\text{eff}}}{d} \quad (15)$$

where  $A_{\text{eff}}$  is the effective area of the patch,  $d$  is the substrate thickness, and  $\epsilon_r$  is the relative permittivity of the dielectric. Considering the dc permittivity range relevant to this study, the estimated capacitance of the LC layer ranges from approximately 561.9 to 786.6 fF. To account for the finite size of the bottom electrode, a correction factor  $\eta = 0.9$  is applied. Under this assumption, the corrected effective capacitance is reduced, yielding a range of approximately 505.7–708.0 fF. Since this value is smaller than the total capacitance of the circuit, variations in the dielectric constant do not significantly affect the overall time constant. The LC used in this study has been experimentally validated for stable operation within a certain temperature range in [18], which confirms reliability under our operating conditions.

### C. Memory Effects on Reconfiguration Speeds

LC materials inherently exhibit elastic relaxation delay and weak ionic polarization, which together give rise to memory effects. Memory effects are a critical issue in LCs, since the intrinsic viscosity and elastic properties of LC materials determine the settling time of molecular reorientation, which is typically slower than that of other tunable devices. In addition, residual charges trapped at the alignment layer can further influence the relaxation time.

First, ionic or molecular residues may accumulate at the alignment layer, where impurity ions or charges in the LC bulk give rise to a residual electric field. The LC remains

in a distorted state until the accumulated charges are fully discharged. Second, there is the delay associated with elastic relaxation. Once mechanically distorted by the applied electric field, the LC directors require a finite time to return to their equilibrium state, governed by the viscosity and elastic constants. As a result, the overall settling time of the LC is characterized by the rise time and decay time, as expressed in the following equations [29]:

$$\tau_{\text{on}} = \left(\frac{h}{\pi}\right)^2 \frac{\gamma}{K_{\text{eff}}} \left(\frac{1}{(V/V_{\text{th}})^2 - 1}\right) \quad (16)$$

$$\tau_{\text{off}} = \left(\frac{h}{\pi}\right)^2 \frac{\gamma}{K_{\text{eff}}} \quad (17)$$

where  $h$ ,  $\gamma$ , and  $K_{\text{eff}}$  represent cell gap, viscosity, and effective elastic constant, respectively. Viscosity and elastic constant are the material characteristics of each LC.  $V_{\text{th}} = \pi(K_{\text{eff}}/(\epsilon_0\Delta\epsilon))^{1/2}$  means Frederiks threshold voltage where directors in the LC cavity start to change at a bias level  $V$  above that of  $V_{\text{th}}$ . The larger the anisotropy  $\Delta\epsilon$  is, the smaller the threshold voltage is. From these equations, the rise time can be reduced by decreasing the LC cell gap or by increasing the bias voltage level. However, the decay time can only be reduced by decreasing the LC cell gap, which fundamentally limits the switching speed of LC-based antennas and must be overcome for practical reconfigurable devices. The measurement of LC switching dynamics has been well established in [23]. We emphasize that the governing factors for reconfiguration time are primarily the rise and decay times, rather than ionic residue, because the effective surface area of the alignment layer is negligible compared to the bulk volume; therefore, such charge-related effects are not pronounced at RF frequencies.

It is worth noting that acceleration techniques such as voltage overdrive, dual-frequency LC mixtures, or the use of ferroelectric LC have been reported to reduce the effective switching time by one or two orders of magnitude [30]. These approaches, while outside the scope of the present work, represent potential pathways to overcome the intrinsic decay-time limitation.

#### D. Power Consumption

This section addresses the power consumption characteristics of the proposed LC-based RIS module. While numerous studies have investigated LC-based or other reconfigurable RAs for RIS hardware implementation, most have not reported detailed power consumption metrics. Recently, modeling efforts for RIS power consumption have been conducted for architecture utilizing p-i-n diodes, varactors, and RF switches [19], [20].

However, comprehensive power analysis for LC-based RAs remains limited in the literature. When evaluating the power consumption of a reconfigurable RA, the power drawn by the bias circuit plays a significant role.

Fig. 16 illustrates the operation diagram of the proposed RIS, which is controlled by bias pulses generated by a customized bias circuit. Based on the code book, desired beamforming can be achieved by supplying bias pulses from

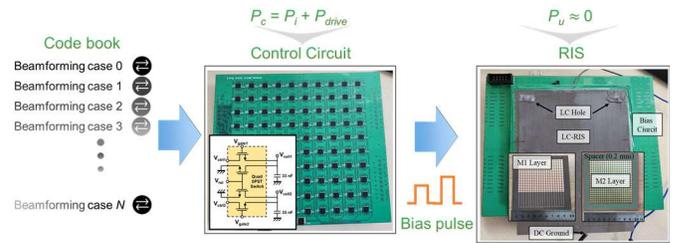


Fig. 16. Operation diagram of the proposed RIS controlled by bias pulses.

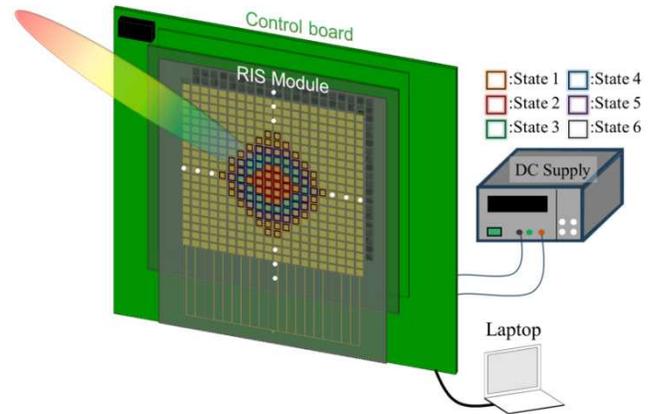


Fig. 17. Power-consumption measurement setup for the RIS hardware and control system.

the bias circuit. The control circuit comprises digital-to-analog converters (DACs) with buffer amplifiers, transistors, and capacitors. The power consumption of the bias circuit is expressed as (6). This can be mathematically expressed as

$$P_c = P_i + P_{\text{drive}} + P_u. \quad (18)$$

Here,  $P_i$  denotes the idling power required to keep the circuit operational,  $P_{\text{drive}}$  represents the variable power consumed by the tunable components during active operation, and  $P_u$  refers to the power dissipated in each RIS unit cell. Based on the power consumption model presented in [19], the total power consumption  $P_{\text{total\_drive}}$  can be further expanded as

$$P_{\text{total}} = P_i + (\mathbb{I}_v + \mathbb{I}_h) \left[ \frac{N}{N_g \cdot N_s} \right] \cdot P_{\text{drive}}. \quad (19)$$

Here,  $N$ ,  $N_g$ , and  $N_s$  denote the total number of RIS unit cells, the number of cells grouped under the same control signal, and the total number of independent control signals, respectively. The indices  $\mathbb{I}_v$  and  $\mathbb{I}_h$  represent the vertical and horizontal polarization states, taking binary values (0 or 1) depending on the polarization configuration used in the system.

Fig. 17 illustrates the procedure for extracting the power consumption using a dc power supply. When a codebook or a uniform bias voltage is applied across all unit cells, the supply current is directly indicated by the power source, allowing straightforward calculation of the total consumed power. If the dc supply is connected without applying any voltage to the unit cells, the measured power corresponds to the idling power of the bias circuit. In the proposed RIS module, the number of cells is  $N = 400$ , and the number of control signals is  $N_s = 40$ , while  $N_g$  depends on the specific beamforming

TABLE III  
POWER CONSUMPTION

		$P_i$ (W)	$P_{total\ drive}$ (W)	$P_{total}$ (W)
Voltage	0 V	1.675	0	1.675
	5 V	1.675	0.45	2.125
	10 V	1.675	0.5	2.15
Beamforming	0°	1.675	0.375	2.05
	10°	1.675	0.425	2.1
	20°	1.675	0.275	1.95
	30°	1.675	0.395	2.07
	0°	1.675	0.375	2.05

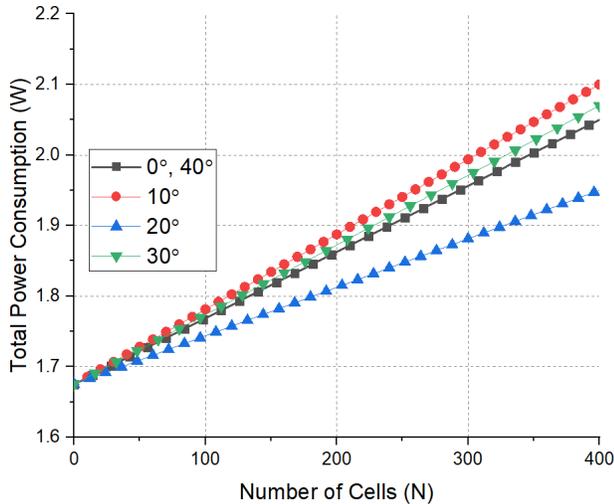


Fig. 18. Power consumption extraction for each beamforming case.

configuration employed. For instance, the instantaneous power consumption during active biasing can reach up to 2.05 W. However, since the biasing is applied in short pulses, not continuously, the actual energy consumption is much lower. Once the beamforming state is configured, the dc supply can be turned off, and the average power consumption drops significantly, as the duration of the bias frame (i.e., the period during which all unit cells are actively biased) is typically less than one second.

Table III summarizes the measured power consumption across supply voltages from 0 to 10 V and various beamforming states. The maximum value of 2.15 W was observed when 10 V bias pulses were simultaneously applied to all 400 unit cells. This figure consists of the idling power of the bias circuit (1.675 W, primarily from DACs, buffer amplifiers, and digital control components) and the transient drive power required to charge the unit-cell storage capacitors ( $\sim 0.45$  W). Once the desired beam state is configured, the switches remain off and the capacitors retain the stored charge, reducing the steady-state power consumption of the RIS array itself to a negligible level. For comparison, RIS structures based on varactors and p-i-n diodes consume approximately 180 and 10 W, respectively, for a  $20 \times 20$  cell configuration [19], mainly due to their biasing architectures and additional internal components.

Fig. 18 plots the total power consumption as a function of the number of cells, extrapolated using the power scaling model from [19]. In large-scale deployments, such as a  $100 \times 100$  RIS array, the proposed architecture would

require only 200 bias nodes due to the active addressing scheme, and the maximum power required for beamforming would be 12.3 W. This power level is comparable to that of typical consumer electronics—for instance, a television ( $\sim 100$  W) or a microwave oven ( $\sim 700$  W)—making the proposed LC-based RIS highly energy-efficient and scalable for practical wireless infrastructure applications.

#### IV. CONCLUSION

This article proposed a low-power LC-based RIS module capable of beam-holding without continuous power supply. By integrating switches and capacitors into the bias circuit, the system enables quasi-permanent beamforming with minimal energy consumption. An active addressing scheme requiring only  $2N$  control lines for an  $N \times N$  array was implemented to reduce complexity. A  $20 \times 20$  prototype was fabricated, and antenna measurements demonstrated 2-D beam-scanning with up to  $\pm 40^\circ$  coverage and 23.7% aperture efficiency. The LC-based design achieved a phase shift of over  $200^\circ$  with only 2.15 W peak power during beamforming. After beamforming, the holding power dropped to near-zero power consumption due to the capacitor-based retention. Compared to p-i-n and varactor-based RISs (10–180 W), the proposed module exhibits superior energy efficiency. Scalability analysis showed that even a  $100 \times 100$  RIS array would require just 12.3 W. These results validate the feasibility of the LC-based RIS for FWA and other low-power, infrastructure-free communication scenarios.

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